# RMS Detector of Multiharmonic Signals

Predrag B. Petrović

**This paper presents a new realization of the implicit root-mean-square (RMS) detector, employing three second-generation current conveyors and MOS transistors. The proposed circuit can be applied in measuring the RMS value of complex, periodic signals, represented in the form of the Fourier series. To verify the theoretical analysis, circuit Simulation Program with Integrated Circuit Emphasis simulations and experiment results are included, showing agreement with the theory.**

**Keywords: RMS detector, multiharmonic, current conveyors, MOSFET, band-limited signals, simulation, experiment results.**

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## I. Introduction

Root-mean-square (RMS) power detectors are used in telecommunication and measurement systems, for example, for transmitter power control, in multitone testing, and for electromagnetic interference (EMI) measurement [1]. Generally, RMS power detection is more useful than peak power detection because RMS power detection is a consistent and standard method for measuring and comparing dynamic signals independent of waveform shape [2]. Diverse methods and circuits have been developed to enable the precise measurement of the effective value of the processed signals, such as sampling [3], the Monte Carlo method [4], and the wavelet transform [5]. Design techniques based on bipolar dynamic translinear circuits have been proposed to implement true RMS-to-DC converters [6]. Translinear-based detectors have limited bandwidth compared to thermal-based or diode-based detectors (due to input interference) [7]. Although the literature abounds with papers containing detailed accounts of the operation of the implicit RMS converter [8], [9], this converter type cannot adequately process and measure the effective value of a complex, multiharmonic, and band-limited input signal.

It goes without saying that the use of current-mode active devices has some advantages, such as greater linearity, wider bandwidth, larger dynamic range, and less power consumption, compared to their voltage counterparts, operational amplifiers. The second-generation current conveyors (CCIIs) [10] have been used in numerous applications, such as universal filters, inductor simulators, capacitance multipliers, oscillators, and full-wave rectifiers [11]. In this paper, a novel circuit for measuring the RMS value of complex, band-limited signals, based on usage of CCIIs, is presented. In terms of frequency range, the proposed circuit operation covers a wide range of as many as five decades, with increased linearity and

  

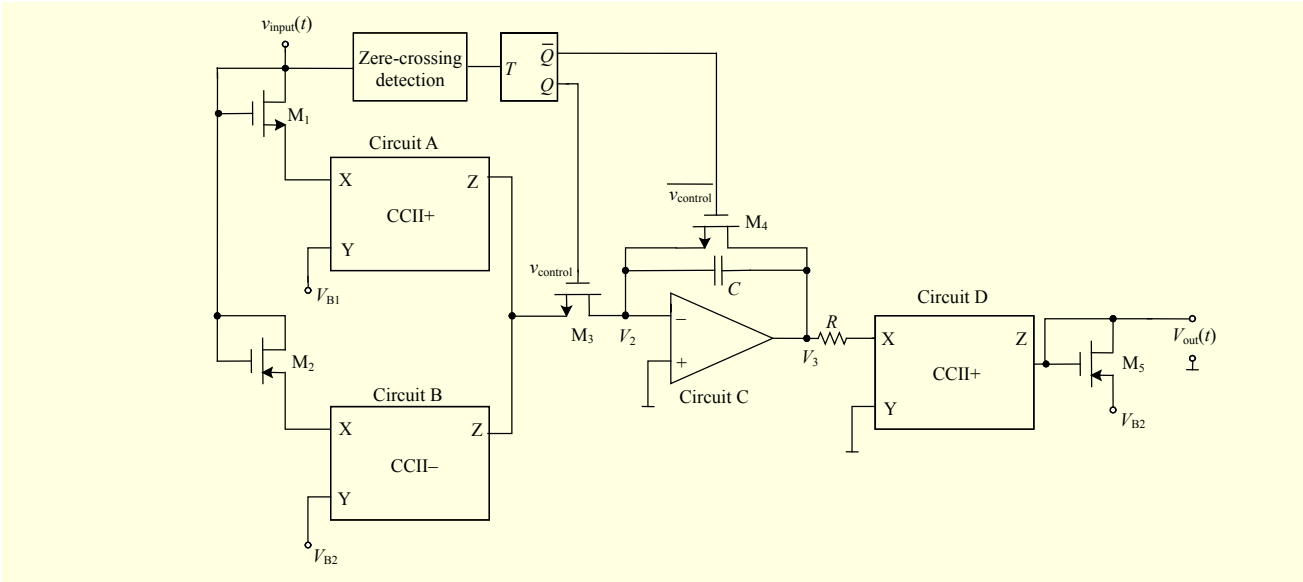


Fig. 1. Proposed realization of implicit RMS detector.

precision in determining the effective value. In addition, the circuit has few passive components, which makes it very suitable for the IC implementation. Simulation Program with Integrated Circuit Emphasis (SPICE) simulations and experiment results are also given to demonstrate the performance of the proposed circuit.

## II. Proposed RMS Detector Circuit

The proposed circuit for measuring the RMS value of a multiharmonic, band-limited input signal is shown in Fig. 1. In contrast to the circuit described in [12], the proposed circuit is based on a single output (SO) CCII, which can deliver more impressive performance and has a simpler internal circuit structure for measuring. In addition, the proposed circuit offers a fully defined structure for generating the control signals that manage RMS detectors. The proposed circuit excludes single pole double-throw analogous switches [12], which affect the precision in generating the effective value of the input signal. The proposed solution makes possible any later analyses of probable sources of errors occurring during the processing of the complex-periodical input signal. As shown in Fig. 1, the circuit consists of three diode-connected MOS transistors (high-quality diodes) and an integrator, together with three CCIIs. The NMOS transistor $M_1$ has the threshold voltage $V_{Tn}\geq 0$. The identical PMOS transistors ($M_2$, $M_5$) have the threshold voltage $V_{Tp}\leq 0$. The Y ports of the CCs are biased at the threshold voltages of the MOS transistors as $V_{B1}=-V_{Tn}$ and $V_{B2}=-V_{Tp}$ (for CCs, $v_x=v_y$). The bulk of all of the MOS transistors is connected to their sources. This arrangement yields a desirable performance of the proposed circuit in twin tube-technology implementations, as well as in discrete-component implementations. If N-well CMOS technology is used in the realization of the proposed detector, threshold voltages of the MOS transistors can deviate from their nominal value in reality. It is for this reason that we can use techniques proposed for the realization of some other circuits [13]-[15]. By introducing self-biasing, it is possible to avoid the necessity for external biasing and entailing requirements for special bandgap bias circuits; since all the internal bias voltages and currents are generated from each other, the bias levels are completely determined by the operating conditions.

If we assume that the input voltage signal $v_{input}(t)$ presupposes an arbitrary band content that can be represented as a sum of its Fourier components, then

$$v_{\text{input}}(t)=\sum_{r=0}^{N}V_r\sin(r\omega t+\psi_r), \tag{1}$$

where $\omega=2\pi f$ stands for the angular frequency, $V_r$ is the amplitude value of the $r$-th harmonic, $\psi_r$ is the phase angle of the $r$-th harmonic of the voltage, and $N$ is the number of the highest harmonic components of the voltage signal.

If $v_{input}(t)$ is positive, the current is conducted through the NMOS transistor $M_1$ to the output. However, if $v_{input}(t)$ is negative, it is the PMOS transistor $M_2$ that conducts the current to the output, that is,

$$\begin{aligned} I_{D1}&=\frac{k_n}{2}(v_{GS1}-V_{Tn})^2=\frac{k_n}{2}v_{\text{input}}^2(t);\ \text{for } v_{\text{input}}(t)>0,\\ I_{D2}&=\frac{k_p}{2}v_{\text{input}}^2(t);\ \text{for } v_{\text{input}}(t)<0, \end{aligned} \tag{2}$$

where $I_{D1}$ and $I_{D2}$ represent the drain currents of the $M_1$ and $M_2$

transistors, respectively. The parameters $k_n$ and $k_p$ are the transconductance parameters of the NMOS and PMOS transistors, respectively. The NMOS and PMOS transistors conduct in opposite halves of the input signal, and CCII+ changes the polarity of the negative input cycles to a positive one at the output. For CCII+, $i_X=i_Z$, while for CCII–, $i_X=-i_Z$. Therefore, the square of the input voltage is obtained at the $M_5$ (after performing integration by the means of the integrator, Circuit C in Fig. 1), whose transconductance is set to nullify the constant from the previous stages. Assume that

$$k = k_n = k_p, \tag{3}$$

for the transistors $M_1$, $M_2$, and $M_5$. It follows that

$$I_{D1} + I_{D2} = \frac{k}{2} v_{input}^2(t). \tag{4}$$

The above represents the total current in the node at the output of the first CCII (Circuit A in Fig. 1). The current formed in this manner passes through the $M_3$ transistor, reaching the integrator (Circuit C in Fig. 1). It ought to be noted here that transistors $M_3$ and $M_4$ cannot lead simultaneously, as their respective positions depend on the value of the control signal $v_{control}$. The voltage at the output of the integrator thus becomes

$$V_3 = \frac{1}{C}\frac{k}{2}\int_0^{t_1} v_{input}^2(\tau)\,d\tau. \tag{5}$$

The voltage formed in this way generates current that is then equalized with the current of the transistor $M_5$ by means of the CCII+ (Circuit D in Fig. 1). It follows that

$$I_{D5} = \frac{1}{RC}\frac{k}{2}\int_0^{t_1} v_{input}^2(\tau)\,d\tau = \frac{k}{2}V_{out}^2(t_1). \tag{6}$$

The above renders the following:

$$V_{out}(t_1) = \sqrt{\frac{1}{RC}\int_0^{t_1} v_{input}^2(\tau)\,d\tau}. \tag{7}$$

If we adjust $RC=T$ and $t_1=T$, where $T$ is the period of the input complex signal, it is clear that (7) represents a definition expression for the calculation of the effective value of the input complex voltage signal. It is important to note that (7) is valid for any input signal (sine-, square-, triangular-wave) whose $T$ period is known.

To enable higher flexibility and adaptability of the proposed RMS detector regarding equalizing the time constant ($RC$) of the integration circuit and the period of the processed input signal; the integrator Circuit C in Fig. 1 can be substituted with an integrator with a tunable time constant [16], [17].

The input voltage signal can possess a DC component, and still yield a correct calculation of the effective value. The performance of the proposed detector is controlled by means of the transistors $M_3$ and $M_4$ as well as the signal $v_{control}$. The transistor $M_3$ ought to be conductive at the interval that equals the $T$ of the input signal, which is the same interval when the transistor $M_4$ is not conductive. The control signal $v_{control}$ can be generated in accordance with the detected zero-crossing of the input signal, which is the object of the processing. In the period in which the $M_3$ does not conduct, the condenser $C$ is discharged to the zero voltage, thus preparing the integrator for the next round of the charging process. On the basis of the detected zero-crossing of the processed signal, edge-triggering of the T flip-flop is performed, which at its output generates a control signal $v_{control}$.

It is also possible to process any input signal that possesses interharmonic and subharmonic components, provided that the period of such a signal is known [18]. The proposed circuit is very appropriate for hardware realization in integrated technology and possesses a much simpler structure than circuits described in [8], [12], [19], [20]. Passive components ($R$ and $C$) would be an additional, external IC circuit, not raising the chip area. In the proposed circuit, rectification of the input signal is not performed by diodes, and it therefore has fewer ripples compared with the known diode circuits. It is also possible to perform low-voltage (below diode threshold level) processing using the proposed circuit.

## III. Error Analysis

It is obvious that (7) is valid under the ideal condition:

$$\begin{aligned} &RC = t_1 = T;\ \ \alpha_1 = \alpha_2 = \alpha_3 = 1;\ \ k_p / k_n = 1, \\ &\lambda_i v_{DSi} = 0,\ \ i = [1,2,5], \end{aligned} \tag{8}$$

where $\lambda$, the channel-length modulation parameter, models the current dependence on drain voltage due to the Early effect or channel length modulation, and $\alpha_i$ represents the current transfer gains of the CCIIs [10]. In the proposed circuit, $v_{DSi}=v_{GSi}$. Given the non-ideal current gains of the CCIIs (ignoring the effects of voltage gains), the output voltage $V_{out}$ (Fig. 1) in the non-ideal condition becomes

$$\begin{aligned} &V_{out}(t_1) \\ &= \sqrt{\frac{\alpha_3}{(1+\lambda_5 v_{DS5})RC}\int_0^{t_1}\left(\begin{array}{l}\alpha_1 v_{input}^2(\tau)_+(1+\lambda_1 v_{DS1}) + \\ +\alpha_2\frac{k_p}{k_n}v_{input}^2(\tau)_-(1+\lambda_2 v_{DS2})\end{array}\right)d\tau}, \\ &v_{input}(t)_+ = \begin{cases} v_{input}(t), & \text{for } v_{input}(t) > 0, \\ 0, & \text{otherwise}, \end{cases} \\ &v_{input}(t)_- = \begin{cases} v_{input}(t), & \text{for } v_{input}(t) < 0, \\ 0, & \text{otherwise}. \end{cases} \end{aligned} \tag{9}$$

Table 1. Uncertainty budget (size of error in determining RMS value of input voltage, which occurs as consequence of non-ideal nature of components applied in circuit proposed in Fig. 1).

| Paramet. | Eval. grade | Uncert. (%) | Type | Distrib. | Sensitiv. | Contr. (%) |
|---|---|---|---|---|---|---|
| $RC$ (ms) | 0.020 | 0.58 | B | Unif. | –0.50 | 0.15 |
| $t_1$ (ms) | 0.020 | 0.58 | B | Hiper. | (0 - 3.0)* | 0.29 |
| $\alpha_i$ | 1 | 0.58 | B | Unif. | (0 - 0.50)* | 0.15 |
| $k_p/k_n$ | 0 | 0.58 | B | Unif. | (0 - 0.50)* | 0.15 |
| $\lambda_i v_{DSi}$ | 1 | 0.58 | B | Unif. | (0 - 0.50)* | 0.15 |
| $e$ | 0 | | | | | 0.82 |

*Sensitivity to changes in certain factors is function of form of input voltage;

*For practical reasons, uncertainty of parameters $\lambda_i v_{DSi}$ has been expressed in percentages of one.

If electronically tunable CCIIs (ECCIIs) [21] are employed instead of CCIIs for the proposed circuit, the parameters $\alpha_1$, $\alpha_2$, and $\alpha_3$ can be used as tools to change the values of the input voltages or to compensate for the error in their values. It is observed in (9) that the square of the negative cycle of the input signal is multiplied by $k_p/k_n$ instead of unity. Fortunately, using ECCIIs, $\alpha_1\alpha_3=\alpha_2\alpha_3 k_p/k_n=1$ can be adjusted. For any divergence in the value of the parameter in relation to its nominal value, it is possible to determine the value of the output voltage and calculate the ensuing error.

The values shown in Table 1 correspond to the case in which all the parameters of interest are known within the limits of ±1% in relation to their nominal values, based on a uniform distribution of probability, that is, the *uncertainty budget*, which is based on the procedures described in GUM [22]. Further on, the input voltage is constructed in such a manner that the DC component of the amplitude and that of the harmonic are randomly positioned (uniform distribution). If it is known that for certain parameters these are not real limits, it is easy to make corresponding corrections in the values. The specific nature of the uncertainty budget set in this manner is reflected in the fact that it is not possible to establish exact values for sensitivity for certain parameters since the concrete values are dependent on the form of the input voltage. The sensitivity to these parameters is represented as the interval of possible values.

If the upper bounds of such intervals are taken as a base for calculation of the combined measuring uncertainties, this would result in a probably unjustified increase of the measurement uncertainty, whereby the calculation shows that the standard measurement uncertainty equals 1.9%, that is, that the expanded uncertainty (for a coverage factor $k = 2$) amounts to 3.8%. However, it is not possible to determine to what extent this would be unjustified by using the usual procedures of

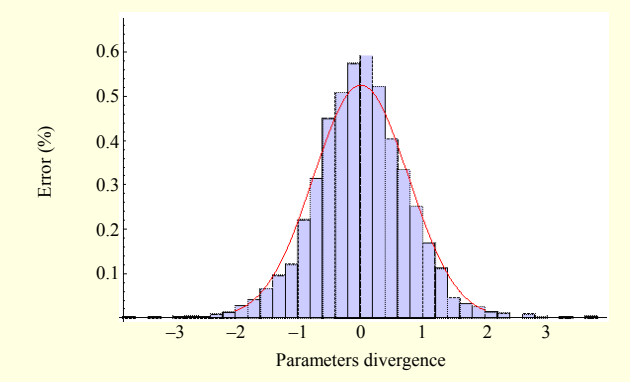


Fig. 2. Distribution of errors reflecting divergence in value of parameters from their nominal values.

determining the measurement uncertainty as described in GUM [22]. It is equally possible, for example, to make use of the mean values of sensitivity. By assuming a uniform distribution of the sensitivity (of the first error derivatives per parameter), that is, a distribution that is essentially hyperbolic, as has been shown by the experiments, for the sensitivity to a $t_1$ change in the parameter, this may be logical; however, it will always remain unknown how far we are from a realistic estimate. If this approach is applied, standard measurement uncertainty equaling 0.82% is obtained, that is, an expanded uncertainty (for the coverage factor $k = 2$) amounting to 1.6%.

The evaluation of uncertainty in the results of measuring obtained through a simulation of the impact made by variations of all the parameters of interest can be based on one of the methods known as the Monte Carlo method. It is expected that such a method offers a more realistic evaluation of uncertainty, given the fact that it does not imply any assumptions, either regarding the distribution of the output value, the error in the measuring results, or the distributions of the sensitivity values. Figure 2 shows the result of implementing the Monte Carlo variants under the identical assumptions as before (the simulations were performed assuming that the input voltage possesses a DC component and ten harmonics, with randomly chosen amplitudes and phases).

The expanded measurement uncertainty obtained here amounts to 1.5%, and it ought to be compared with the data obtained from the uncertainty budget (3.8%). The number of individual simulations in the presented case is 2,200. The experiments are repeated to include cases in which the input voltage contains interharmonics in addition to harmonics:

$$v_{\text{input}}(t) = V_0 + \sum_{i=1}^{n} V_i \sin(i\omega t + \varphi_i) + \sum_{i=1}^{n-1} V_i' \sin\left(\frac{i}{n}\omega t + \varphi_i'\right) + \sum_{i=2}^{n-1} V_i'' \sin\left(\frac{n}{i}\omega t + \varphi_i''\right). \quad (10)$$

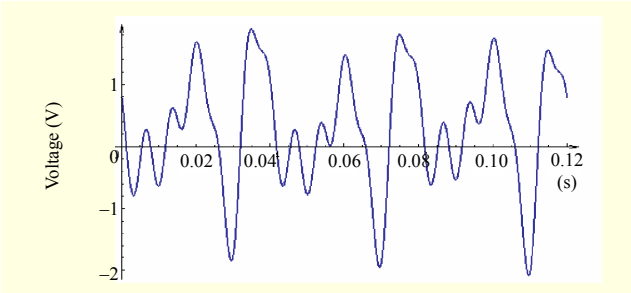


Fig. 3. Example of input signal with interharmonics.

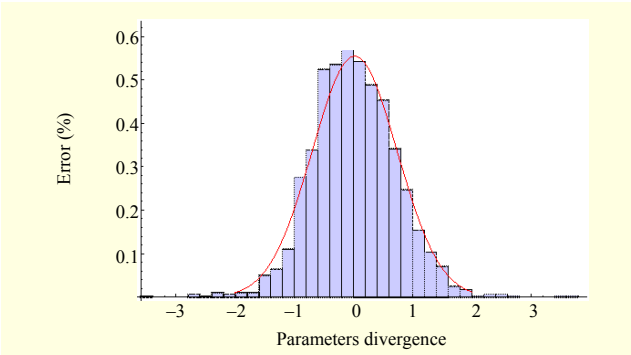


Fig. 4. Distribution of errors reflecting divergence in value of parameters from their nominal values in the case of processing the signal shown in Fig. 3.

For the purpose of simplification, $n=3$ is applied. Parameters $V_0$, $V_i'$, $V_i''$, $\varphi_i$, $\varphi_i'$, and $\varphi_i''$ gain random values within the range from 0 to 1, that is, within the range from 0 to $2\pi$. An example of one of the signals with a base frequency of 50 Hz is shown in Fig. 3. Figure 4 shows the result of implementing the signal shown in Fig. 3. The number of individual simulations in the presented case is 1,500. The measurement uncertainty obtained here amounts to 1.4%. It can therefore be concluded that the system functions equally well when interharmonics are added to the input voltage.

## IV. Simulation and Experiment Results

To check the performance of the proposed RMS detector, a simulation of its operation is conducted in SPICE. The MOS transistors represented in Fig. 1 are simulated based on the 0.35-µm Taiwan Semiconductor Manufacturing Company, Limited (TSMC) CMOS technology, with ±1.5 V DC power supply voltages [23]. AD844-type CCs (CCII+) with ±5 V DC power supply voltages are used for the circuit implementation. The CCII– is realized by using two serially connected CCII+. In addition, $V_{B1}$=–0.544 V and $V_{B2}$=0.714 V are chosen. The simulation is conducted using 0.35-µm transistors to show that the proposed solution would work for fully integrated systems. This approach was used in recently published papers dealing with relative issues [11], [12]. During the simulation, the parameters of the input signal corresponded to the values given in Table 2. The input voltage is a multiharmonic sinusoidal signal, as assumed in (1), with a fundamental frequency of $f=1/T=50$ Hz.

Table 2. Simulation results of proposed RMS detector in SPICE.

| Amplitude (V) | Phase (rad) | Obtained RMS value | Relative error of measured RMS value of voltage (%) |
|---|---|---|---|
| $V_1$=0.5; $V_2$=0.3 | $\psi_1$=0; $\psi_2=\pi$ | 0.4118 | 0.12 |
| $V_1$=0.3; $V_2$=0.25; $V_3$=0; $V_4$=0.12; $V_5$=0.05 | $\psi_1$=0; $\psi_2=\pi/2$; $\psi_3$=0; $\psi_4=\pi/3$; $\psi_5=\pi$ | 0.2906 | 0.13 |
| $V_1$=0.5; $V_2$=0.46; $V_3$=0.35 | $\psi_1$=0, $\psi_2=\pi$, $\psi_3=\pi/6$ | 0.5398 | 0.11 |
| $V_1$=0.4; $V_2$=0.3; $V_3$=0.25; $V_4$=0; $V_5$=0.2; $V_6$=0.12; $V_7$=0.08 | $\psi_1$=0; $\psi_2=\pi/4$; $\psi_3=\pi/5$; $\psi_4$=0; $\psi_5=\pi/7$; $\psi_6$=0; $\psi_7=\pi$ | 0.4314 | 0.14 |
| $V_1$=0.5; $V_2$=0; $V_3$=0.35; $V_4$=0.2; $V_5$=0; $V_6$=0.12; $V_7$=0.1; $V_8$=0; $V_9$=0.1 | $\psi_1$=0; $\psi_2$=0; $\psi_3=\pi/12$; $\psi_4=\pi$, $\psi_5$=0; $\psi_6=\pi/6$; $\psi_7=\pi$, $\psi_8$=0; $\psi_9=\pi/8$ | 0.4721 | 0.12 |

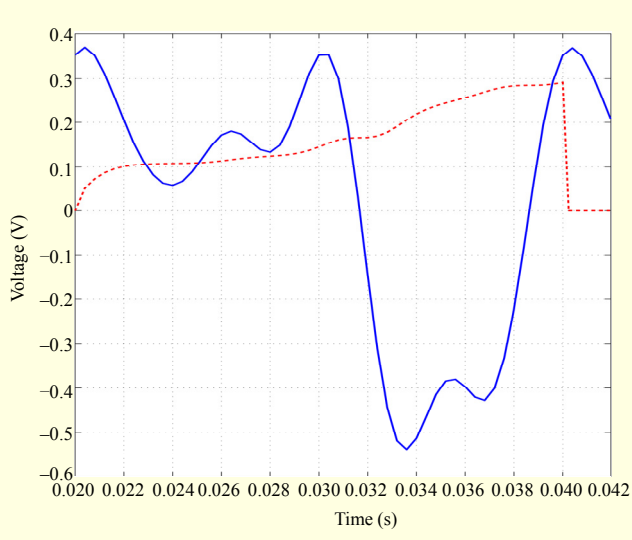


Fig. 5. Time-domain response of proposed RMS detector for multiharmonic sine input signal.

Figure 5 presents the waveform of the input multiharmonic sine signal (primarily highlighting the parameters in the second row of Table 2) along with the signal at the output of the circuit, shown in Fig. 1 (voltage $V_{out}(t)$). As shown in the figure, the value of the signal at the output of the proposed circuit gains the effective value that the processed input signal has at the end of its period (interval length of 20 ms). After the reading of the value, condenser $C$ is discharged by conducting transistor $M_4$,

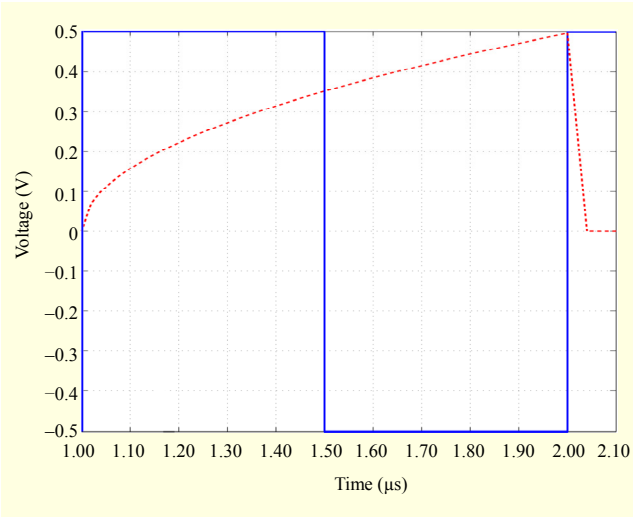


Fig. 6. Time-domain response of proposed RMS detector for square-wave input signal.

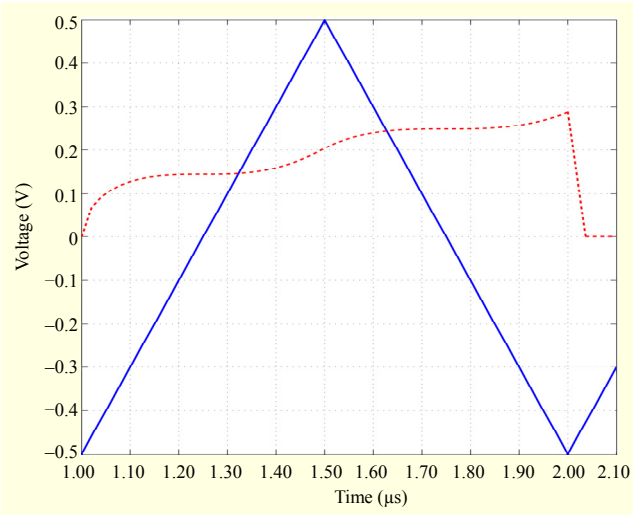


Fig. 7. Time-domain response of proposed RMS detector for triangular-wave input signal.

whereby the circuit assumes the position that allows calculation of the effective value of the processed input signal.

Time-domain responses of the proposed RMS detector for square- and triangular-wave signals are depicted in Figs. 6 and 7, respectively. In these checks, the signals show a 0.5-V peak value and a frequency of 1 MHz. As can be seen in Figs. 5, 6, and 7, it is clear that the theoretical principle sustains the operation at both very low (for applications in power systems) and high frequencies, higher than for circuits proposed in [20], thus confirming that the proposed method is robust against the frequency variation.

All the presented results of the simulation checks (Table 2 and Figs. 5, 6, and 7) confirm the possibility of a highly-precise determination of the RMS value of the input multiharmonic

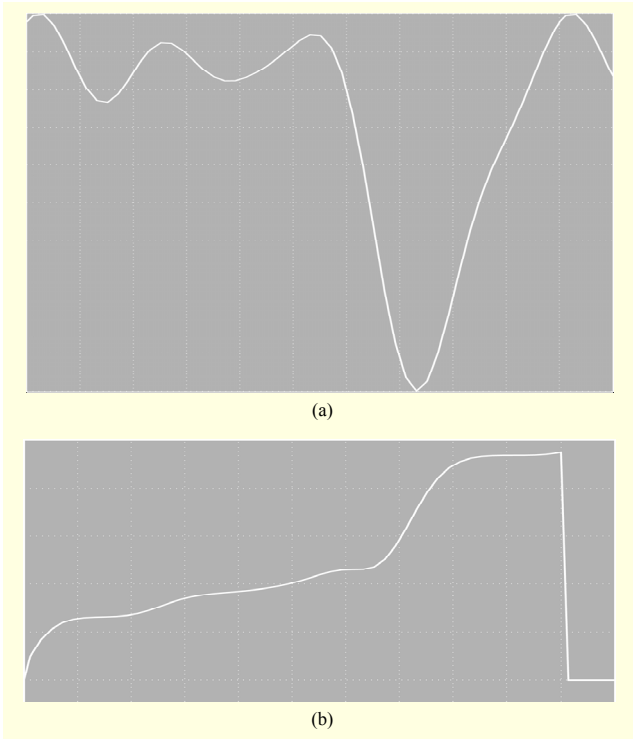


Fig. 8. Experiment results for the RMS detector in Fig. 1 for an input signal defined in (11) (vertical scale: 0.2 V/division; horizontal scale: 10 μs/division). (a) Input multiharmonic sine signal. (b) Output RMS signal.

signal by using the proposed circuit. The margin of error in calculating the RMS value of multiharmonic signals is smaller than the respective margins of error in the detectors proposed in [6], [9], [12], [19], [24], and the structure of the proposed circuit is much simpler. The slight difference between the ideal and simulated responses stems mainly from the parasitic impedances and non-ideal gains of the CCs.

## 1. Experiment Results

The experimental test for the RMS detector shown in Fig. 1 is performed by using CD 4007 MOS array transistors and AD844 operational amplifiers (Analog Devices, Inc.) to realize the CCIIs and the integrator. The DC power supply for AD844s is ±15 V, the biasing voltage $V_{B1}$ is equal to –2 V (negative of the threshold voltage of the deployed NMOS transistors), and $V_{B2}$ is equal to +1.5 V (for PMOS transistors).

The input voltage signal in the form

$$\begin{aligned} v_{\text{input}}(t) = {} & 1\sin(2\pi ft) + 0.82\sin\left(4\pi ft + \pi/2\right) \\ & + 0.45\sin(6\pi ft + \pi) + 0.2\sin(8\pi ft) \\ & + 0.15\sin\left(10\pi ft + \pi/4\right), \end{aligned} \tag{11}$$

where $f$=10 kHz, is applied to the RMS detector. The value of

the time constant of the integration circuit is adjusted to correspond to $RC$=0.1 ms. The above-mentioned input signal is generated by using acquisition card NI ELVIS/PCI-6251 Bundle (National Instruments).

Figure 8(a) represents the waveform of the input signal defined by (11), and Fig. 8(b) shows the waveform of the output voltage of the proposed RMS detector. The voltage at the end of the $T$ period reaches the effective values of the processed signal (11). The read-out value of the RMS voltage is approximately 0.983 V. The difference between the experimental and theoretical values of RMS shown in Fig. 8(b) may be due to the deviation of the design parameters, such as the $R$, $C$, and input impendence of the ICs used in the circuit from its experimental values.

## V. Conclusion

This paper presented a novel RMS detector configuration that can be used for determining the effective value of a complex, periodical, band-limited input voltage signal. The proposed solution presupposes that computation of the effective value of the processed signal is conducted in full compliance with the definition pattern, which excludes limitations resulting from all the problem realizations made so far [8], [9], [11] and ensures more precise measurement. For its realization, the RMS detector requires only three CCIIs, one OP, and five MOS transistors. The proposed current processing method offers several advantages in integrated circuit implementation. In terms of frequency range, the proposed circuit provides accurate RMS measurements over a frequency range of 50 Hz to 1 MHz. The precision limit of the proposed detector was investigated both theoretically and experimentally and by simulation.

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