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Tunable flux-controlled floating memristor emulator circuits

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Predrag B. Petrović[1] ✉

[1]*Faculty of Technical Sciences, University of Kragujevac, Svetog Save 65, Čačak, Serbia*
✉ *E-mail: predrag.petrovic@ftn.kg.ac.rs*

Abstract: This study proposes two new emulator circuits of floating (grounded) flux-controlled incremental/decremental memristor, based on modified *z*-copy current–voltage differencing transconductance amplifier (VDTA). The circuits use only one VDTA as an active element, a single grounded capacitor and a variable number of grounded resistors, which benefit from the integrated circuit. Furthermore, it can utilise metal–oxide–semiconductor (MOS) capacitance instead of the external capacitor in the circuit. It does not consist of any multiplication circuit block to obtain non-linear behaviour of the memristor. The parameters of the proposed memristor emulator can be tuned electronically by changing the biasing current of the VDTA. Change of the transconductance gain of the VDTA provides an advantage in the form of the externally controllable memristor. Through the simulation program with integrated circuit emphasis (SPICE) simulation which was carried out on the basis of 0.18 μm complementary MOS technology and experimental results using two MAX435 commercial devices as an active element, all theoretical assumptions and conclusions were reached in different operating frequencies, the capacitance value and process corner. The simulation test results have shown that the maximum frequency is 50 MHz.

1 Introduction

Ever since it has been defined as the fourth principal constitutive element [1] establishing the connection between the charge and flux linkage, the memristor grabbed the attention of not only the expert public, but also of people of different backgrounds. In general, memristors are passive, history-dependent, polarised and frequency-dependent circuit elements. The voltage–current curve of memristor shows a pinched hysteresis loop and linear characteristics when applying sinusoidal signals with low and high frequencies, respectively. After its practical implementation was accomplished [2], a wide field for its implementation has opened such as oscillator, chaotic, logic applications, associative learning, a memory circuit and neuromorphic circuit. Not only have emulator circuits solved the availability problem of the memristor, but they have also eliminated certain application problems of physical memristors [2]. For instance, emulator circuits can be tuned for low or high operating frequencies, with various types of memristor emulators being designed in recent years by using different active elements, transistors and analogue–digital circuits, knowing that reaching the memristors as discrete circuit elements is a difficult task involving a number of fabrication problems.

Memristor emulators can be divided into two types according to their structures: floating memristors [3–13] and grounded memristors [14–24], with only certain memristor emulator circuits being suitable for high frequencies in the order of megahertz (MHz) [4, 5, 7, 10, 16, 17, 23, 24]. Some of them can operate with a variable configuration, as one of the solutions proposed here, meaning that it is possible to emulate grounded or floating type of memristor with the same circuits [25–27]. If the memristor emulator circuits are of a grounded type, its application areas are limited in circuit designs, rendering it unsuitable for use as a two-terminal device in more complicated circuits since the grounded restriction places a substantial obstacle on their connectivity with other circuit elements. In addition, emulator circuits of this type, described in the literature so far, utilise a larger number of active and passive elements, which in itself is a limitation to practical implementation, and requires additional circuit blocks to provide floating characteristics. Floating memristor emulator possesses floating terminals and a variable structure that allow the designers to alter the non-linear flux-controlled function only via utilisation of fewer electronic components. To make it successfully emulate a floating memristor, the emulator circuit must satisfy strict parameter matching conditions.

To obtain memristive behaviour from linear circuits is not easy because of the non-linear characteristics of memristors. Active-circuit elements provide advantages in designing complex and non-linear circuit-element patterns. For this reason, various active-circuit-element-based memristor circuits can be found in the literature based on operational amplifier (OpAmp) [3], second-generation current conveyor (CCII) [6, 8, 12, 14, 21, 22], differential difference CCs (DDCC) [5], current backward transconductance amplifier (CBTA) [18], operational transconductance amplifier (OTA) [9, 11, 15, 19, 25] differential voltage–CC transconductance amplifier (DVCCTA) [17], current-feedback OpAmp (CFOA) [13, 20, 26]. Floating memristor emulators using one CCTA, one CCII and few passive elements have been proposed in [4], while the circuits [27] are based on only one CCTA. The active-circuit-based memristors have certain advantages such as electronic tunability of memristance value and easily designed circuits, as well as certain disadvantages such as power consumption, noise and restricted operating frequency, which are due to their structures and operating performances.

Metal–oxide–semiconductor (MOS) transistor level memristor emulators [10, 23, 24], which can be attractive in terms of their structures, have been proposed; however, these circuits require special operating modes of the transistor to provide an unalloyed memristor characteristic. The circuits proposed in [24] are based on a zinc oxide thin film-semiconductor memristor device, which was fabricated by direct-current reactive magnetron sputter.

It is well known that floating memristors have wide application areas compared with the grounded ones, but they have more complex structures, which are avoided in the proposed emulation circuits. The circuits described herein are the first such solutions known in the literature, which are able to provide the emulation of floating memristors based on only one voltage differencing transconductance amplifier (VDTA). This is apparently the principal advantage of the proposed concept, compared with the grounded memristor emulator described in [16].

The configuration of the circuits dealt with in this paper is based on modified *z*-copy VDTA, resembling the emulator circuits described in [7, 16], but having a more compact configuration and

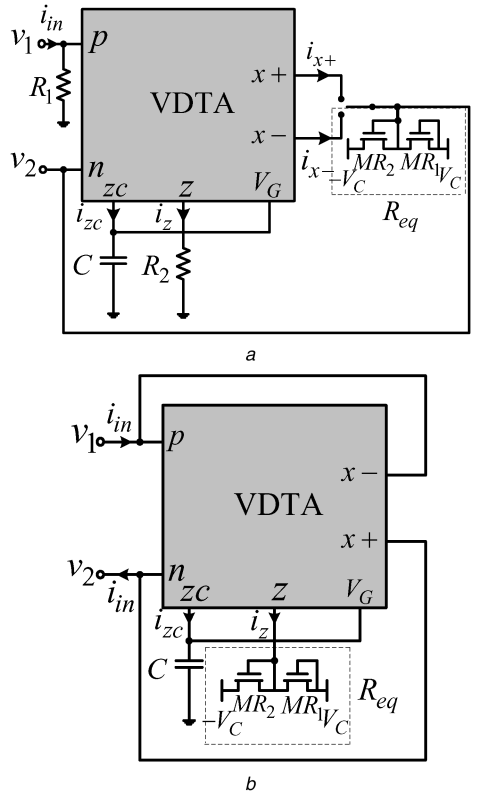

Fig. 1 *Memristor emulator circuits*
(a) Floating incremental/decremental configuration, ***(b)*** Floating/grounded configuration with reduced number of external passive elements

requiring no special multiplier circuit, thus widening the frequency range in which the circuit retains the stipulated performances, while increasing the tunability. Controlling the value of the achieved memductances in the proposed emulator's circuits can be accomplished by changing the transconductance parameter of the used VDTA by a bias current, and changing the value of the electronically controlled resistors (through a control voltage V_C – Fig. 1). In addition, using an extra circuit block such as a multiplier, gives rise to extra power dissipation, complex structure and extra chip area, which was avoided with the proposed realisations. The proposed memristors exhibit a smooth switching mechanism, which can be used in non-linear, chaotic and neuromorphic circuit applications [28, 29], making them more suitable for sensitive memory applications, as well as in resistive-random access memory devices. The new architectures, which are required to transcend the device variability and interconnect scaling bottlenecks of the traditional von-Neumann architecture, should exploit massive parallelism and locally employ memory within the computing elements in a manner similar to biological brains [10]. In addition, an frequency modulation to amplitude modulation convertor can be realised using the proposed memristor emulator circuits [7].

Apart from this, by the means of a simple connection of the second end of the input voltage to the grounding terminal, the proposed variant 2 (Fig. 1*b*) becomes a grounded memristor emulator, a solution proposed in [27]. Considering the number of the deployed transistors, the described circuits can only be compared with the solution [16], while still offering greater controllability than circuit [16], featuring an output range of up to 50 MHz. This maximum operating frequency refers to emulation circuits based on the use of VDTA as an active circuit, while the VDTA circuit itself can offer operation at higher frequencies than 50 MHz [30].

In Table 1, comparison of the proposed emulation circuits here was made with some of the known solutions, especially those that appeared recently. The comparison was performed applying several different criteria – the number of active and passive components, power supply, electronic controllability and power consumption. The power consumption depends on the operating frequency and values specified in Table 1 are referring to the maximum possible consumption in the frequency band in which the emulator circuit maintains the predicted performance. Some of the circuits used for comparison with the solutions described herein use a smaller number of MOS transistors [10, 11, 16], but they are inferior to other performance or configuration-grounded type [16] when compared with the proposed emulator circuits. In addition, the circuit described in [11] requires the operation of two additional P-channel MOS (PMOS) transistors in the sub-threshold region, which in itself represents a limitation in the applications, while the variable resistance in [10] is achieved by operating the transistor in linear (triode) or near-linear region.

2 Proposed emulator circuits

In Fig. 1, the proposed floating (grounded, Fig. 1*b*) incremental/decremental memductance emulators circuits are shown. They consist of only one active component – VDTA, one capacitor and a variable number of grounded (and electronically controlled) resistors.

In the VDTA [7, 16], a differential input voltage (v_p–v_n) obtained with one subtraction at the input stage was transferred by the first transconductance gain (g_{mF}) to the current at the *z*-terminal (i_z). The VDTA is made up of two dependent transconductance gain stages, possessing a dual output transconductance amplifier, so that its transconductance gains can be controlled electronically by biasing voltage or current. The corresponding voltage drop at the *z*-terminal converts to currents at the *x*-terminals by the second transconductance gain (g_{mS}), while a copy of the current i_z is available at the *zc*-terminal (i_{zc}) [7]. All VDTA terminals have high-impedance values.

The terminal relationships of VDTA in the ideal situation can be described as $i_p = i_n = 0$; $i_z = g_{mF}(v_p - v_n)$; $i_{zc} = -g_{mF}(v_p - v_n)$; $i_{x+} = g_{mS}v_z$; and $i_{x-} = -g_{mS}v_z$. Fig. 2 shows the modified complementary MOS (CMOS) realisation of the *z*-copy current VDTA, based on [30] in which the transconductance gain g_{mS} can be varied electronically by voltage V_G. The modification in relation to the VDTA circuit used in [7, 16] is reflected in the use of the M_{12} PMOS transistor gate as a control node, which is conditioned by the polarity of the generated voltage on the capacitor C (Fig. 1). In this way, the use of a special multiplication circuit is avoided in order to achieve the necessary memristive function of the emulator circuit. Also, unlike the circuit described in [16], the suggested solutions used the *zc* (zero copy) port, which fully utilised the potentials of VDTA as an active circuit. An electronically controllable resistor which is composed of only two MOS transistors-R_{eq} can be adjusted through a control voltage V_C as $R_{eq} = (L/W)_{MR1,2}/[2\mu C_{ox}(V_C - V_{Tn})]$, where V_{Tn} represents the threshold voltage of N-channel MOS (NMOS) transistor.

As we can see in Fig. 2, the VDTA is composed of two Arbel–Goldminz transconductances [31], so that the g_{mF} and g_{mS} values (of these two stages) are determined by the output transistor transconductance, which can, respectively, be approximated as [31]

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2}\right) + \left(\frac{g_3 g_4}{g_3 + g_4}\right); \quad g_i = \sqrt{\mu_i C_{ox} W_i I_{BF}/L_i},\ i = 1, \ldots, 4 \tag{1}$$

and also can be controlled by bias current I_{BF} (voltage V_B – Fig. 1). Similarly (see (2))

$$K = \sqrt{\mu_p C_{oxp}(W/2L)_{12}}\left(\frac{\sqrt{\mu_p C_{oxp}(W/L)_5 (W/L)_6}}{\sqrt{(W/L)_5} + \sqrt{(W/L)_6}} + \frac{\sqrt{\mu_p C_{oxp}(W/L)_7 (W/L)_8}}{\sqrt{(W/L)_7} + \sqrt{(W/L)_8}}\right)$$

where μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, K is the gain factor of Arbel–Goldminz cell and W and L are the effective channel width and length of the *i*th MOS transistor, respectively.

Table 1 Comparison of memristor emulator circuits

References	Number of active components	Number of floating passive elements	Number of grounded passive elements	Power supply	Output range	Simulation/ experiment	Floating/ grounded memristor emulator	Electronic controllability	Power consumption	Technology used
[4]	CCTA, CCII-38 MOS transistors	one *R*	two *R*/1 *C*	± 1.5 V	5 MHz	both	floating	no	—	CMOS
[5]	one DDCC and one multiplier	—	one *R*, one *C*	± 1.5 V	1 MHz	simulation	floating	no	—	CMOS
[6]	four CCIIs (AD844) and one multiplier (AD633)	two *R*	three *R*, one *C*	± 10 V	20.2 kHz	both	floating	no	—	bipolar junction transistors (BJT)
[7]	one VDTA, one multiplier−32 MOS transistors	—	two *R*, one *C*	± 0.9 V	2 MHz	both	floating	yes	4.57 mW	CMOS
[10]	one OTA–six MOS transistors	—	one *C*	± 1.2 V	10 MHz	simulation	floating	no	≃22 μW	CMOS
[11]	one OTA, two PMOS	—	one *C*	± 1 V	1 kHz	simulation	floating	no	low	CMOS
[12]	four CCII, three OTA	three *R*	three *R*, one *C*	± 15 V	10 kHz	both	floating	yes	—	BJT
[13]	four CFOA, two diodes	three *R*	one *R*, four *C*	± 10 V	few kHz	—	floating	no	—	BJT
[14]	one CCII (AD844), one multiplier (AD633)	one *R*	one *C*	± 10 V	860 kHz	both	grounded	no	—	BJT
[15]	one MO–OTA, one multiplier	—	one *R*, one *C*	± 1.25 V/ ± 5 V	1 kHz	both	grounded	yes	—	CMOS
[16]	1 VDTA–16 MOS transistors	—	one *C*	± 0.9 V	50 MHz	both	grounded	yes	low	CMOS
[17]	one DVCCTA	one *R*	two *R*, one *C*	NA	50 kHz	simulation	grounded	no	—	CMOS
[18]	one CBTA, one multiplier	one *R*	one *R*, one *C*	± 0.9 V	460 kHz	simulation	grounded	yes	—	—
[19]	four MO–OTA	one *R*	two R, one *C*	± 2.5 V	500 kHz	both	grounded	yes	—	CMOS
[20]	two CFOA, one OTA	—	three *R*, two *C*	± 12 V	2 kHz	experiment	grounded	no	—	BJT
[21]	two CCII, one multiplier, two TL084, two MOS	four *R*	one *R*, one *C*	± 12 V	10 kHz	both	grounded	no	—	BJT
[22]	two CCIIs (AD844), one multiplier (AD633), one buffer (TL082)	one *R*	two *R*, one *C*	± 10 V	1 kHz	both	grounded	no	—	BJT
[23]	seven MOS transistors	—	one *C*	± 0.9 V	50 MHz	both	grounded	no	very low<1 mW	CMOS
[25]	two OTA	—	one *C*	± 1.2 V	8 MHz/ 400 kHz	both	floating/ grounded	yes	—	CMOS
[26]	one CFOA (4/2 AD844, one AD633)	three *R*/one *R*	two *R*, two *C*/three *R*, two *C*	± 10 V	20 kHz	both	floating/ grounded	no	—	CMOS
[27]	CCTA	one *R*, one *C*	one *R*	± 1.5 V/ −1 V	1 MHz	both	grounded/ floating	yes	—	CMOS
this work	1 VDTA, −19 MOS transistors	—	one *C* two *R*, one *C*/one *C*	± 0.9 V	50 MHz	both	floating (grounded)	yes	1.34 mW	CMOS

In the ideal case, for the proposed emulator circuits in Fig. 1*a*, the voltage at the *x*-terminal is defined as

$$v_x = \pm g_{mS} v_z R_{eq} = \pm K\left(V_{DD} - V_G - \left|V_{Tp}\right|\right) g_{mF}(v_1 - v_2) R_2 R_{eq}$$
$$= \pm K g_{mF} R_2 R_{eq}(v_1 - v_2)\left(V_{DD} - \left(-\frac{g_{mF}}{C}\int (v_1 - v_2)\mathrm{d}t\right) - \left|V_{Tp}\right|\right)$$
$$= \pm K g_{mF} R_2 R_{eq}(v_1 - v_2)\left(\frac{g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right) \quad (3)$$

In (3), the sign of the voltage v_x is determined by the direction of the applied current i_x. The polarity of this voltage practically determines the character of the emulator circuit as incremental or decremental. As defined in Fig. 1*a*, this polarity is controlled by an electronic switch, which can be realised in the same technology as the remaining parts of the proposed emulator circuit. The voltage over the two input terminals of circuits in Fig. 1*a* can be thus calculated by

$$v_1 - v_2 = R_1 i_1 \mp v_x$$
$$= R_1 i_1 \mp K g_{mF} R_2 R_{eq}(v_1 - v_2)\left(\frac{g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right) \quad (4)$$

The flux-controlled memductance is defined as

$$W_1(\varphi_{12}) = \frac{1}{R_1}\left(1 \pm K g_{mF} R_2 R_{eq}\left(\frac{g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right)\right) \quad (5)$$

As we can see from Fig. 1*a*, the current in the node with the potential v_2 is determined by the peripheral circuit with which this node is connected, and not by the input current of the node with the potential v_1. For this reason, the circuit from Fig. 1*a* is unable to guarantee the equality of these two currents (the input and output currents of its two terminals). Hence, this emulation circuit should not be used to simulate a canonical memristor [7].

In the case of circuits proposed in Fig. 1*b*, similarly, but on the basis of proposed connections, it follows that:

$$i_{in} = i_{x+} = -i_{x-} = g_{mS} v_z$$
$$= K g_{mF} R_{eq}(v_1 - v_2)\left(\frac{g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right) \quad (6)$$

The memductance of this circuit (Fig. 1*b*) can be defined as

$$W_2(\varphi_{12}) = K g_{mF} R_{eq}\left(\frac{g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right) \quad (7)$$

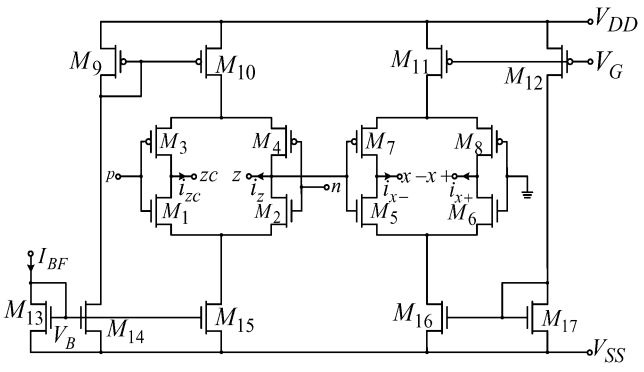

Fig. 2 *CMOS realisation of modified z-copy current VDTA*

It is clear from (7) that a floating incremental/decremental memductance emulator has been obtained. If *n* terminal of VDTA is used according to the positive input terminal of the memristor, the floating incremental memductance emulator is realised. Similarly, if *p* terminal of VDTA is used instead of *n* terminal for the positive input terminal of the memristor, the floating decremental memductance emulator is obtained, meaning that the circuit demonstrates both incremental and decremental behaviours at the same time without changing any circuit topology. It can be observed from (5) and (7) that it consists of linear time variant and invariant parts.

Since VDTA was conceptually composed of two Arbel–Goldminz transconductances cells, each of them, through two stages shown in (5) and (7), defines the memductance values and consequently introduce the possible errors. Considering non-ideal gains of active elements – VDTA [30] (tracking errors), the memductance equation of floating memristors is evaluated as

$$W_1(\varphi_{12}) = \frac{1}{R_1}\left(1 \pm K\beta_{mS}\beta_{mF} g_{mF} R_2 R_{eq}\left(\frac{\beta_{mF} g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right)\right) \quad (8)$$

$$W_2(\varphi_{12}) = K\beta_{mS}\beta_{mF} g_{mF} R_{eq}\left(\frac{\beta_{mF} g_{mF}}{C}\Phi_{in} + V_{DD} - \left|V_{Tp}\right|\right) \quad (9)$$

where β_F and β_S are, respectively, the tracking errors for the first and second stages of the VDTA.

It can be observed from (8) that the linear time variant part of memductance equation of floating memristor alters slightly owing to non-ideal gains of VDTA. So as to overview the frequency characteristic of the presented floating memristor circuits, we used a sinusoidal input voltage which is equal to $V_m \sin(\omega t)$, applying it to its input terminal, where V_m is the maximal amplitude of the voltage signal and ω is $2\pi f$. Input flux (Φ_{in}) is found as

$$\Phi_{in} = \frac{V_m \cos(\omega t)}{\omega} \quad (10)$$

Substituting the input flux in (10) into (8) and (9), memductance equations are obtained depending on the input signal

$$W_1(v_{in}, f) = \frac{1}{R_1}\left(1 \pm K\beta_{mS}\beta_{mF} g_{mF} R_2 R_{eq}\left(\frac{\beta_{mF} g_{mF} V_m}{2\pi C f}\cos(2\pi f t) + V_{DD} - \left|V_{Tp}\right|\right)\right) \quad (11)$$

$$W_2(v_{in}, f) = K\beta_{mS}\beta_{mF} g_{mF} R_{eq}\left(\frac{\beta_{mF} g_{mF} V_m}{2\pi C f}\cos(2\pi f t) + V_{DD} - \left|V_{Tp}\right|\right) \quad (12)$$

It can be easily observed in (11) and (12) that the linear time-invariant resistor depends on *K*, VDTA transconductance parameters, resistors and V_{DD} voltages while a linear time-varying resistor changes with the amplitude of voltage signal, operating frequency, capacitance and the equivalent resistor. Memductances (11) and (12) turn into a linear resistor when the operating frequency, the capacitance value and equivalent resistor value increase. Consequently, the amplitude ratio of the linear time-invariant parts and varying parts is defined as

$$g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right)$$
$$= \sqrt{\mu_p C_{oxp}(W/2L)_{12}}\left(V_{DD} - V_G - \left|V_{Tp}\right|\right)\left(\frac{\sqrt{\mu_n C_{oxn}(W/L)_5 (W/L)_6}}{\sqrt{(W/L)_5} + \sqrt{(W/L)_6}} + \frac{\sqrt{\mu_p C_{oxp}(W/L)_7 (W/L)_8}}{\sqrt{(W/L)_7} + \sqrt{(W/L)_8}}\right) \quad (2)$$
$$= K\left(V_{DD} - V_G - \left|V_{Tp}\right|\right)$$

$$k_1 = \frac{K\beta_{mS}\beta_{mF}^2 g_{mF}^2 R_2 R_{eq} V_m \cos(2\pi f t)}{\left(\frac{1}{R_1} \pm K\beta_{mS}\beta_{mF} g_{mF} R_2 R_{eq}\left(V_{DD} - |V_{Tp}|\right)\right) 2\pi C f} = \frac{1}{\tau_1 f} = \frac{T}{\tau_1} \quad (13)$$

$$k_2 = \frac{\beta_{mF} g_{mF} V_m \cos(2\pi f t)}{(V_{DD} - |V_{Tp}|) 2\pi C f} = \frac{1}{\tau_2 f} = \frac{T}{\tau_2} \quad (14)$$

where τ_1 and τ_2 are the time constants and T is the time period. From (13) and (14), one can deduce that the pinched hysteresis behaviour depends not only on the amplitude-to-frequency ratio of the stimulating signal, but also on the time constant of the emulator circuits itself. On the basis of the two equations above, we can conclude that:

- k_1, $k_2 \to 0$ when $f \to \infty$. Its linear time-invariant conductance dominates the memductance behaviour.
- k_1, $k_2 \to 1$ when $f \to 1/\tau_{1,2}$. The pinched hysteresis loop maximum is achieved.
- k_1, $k_2 \geq 1$ when $f \leq 1/\tau_{1,2}$. The hysteresis loop is lost. This means that T is larger than $\tau_{1,2}$.

A situation when f is fixed and V_m is varied reveals that:

- k_1, $k_2 \to 0$ when V_m decreases. Its linear time-invariant conductance also dominates the memductance behaviour.
- k_1, $k_2 \to 1$ when V_m is monotonically increased. The pinched hysteresis loop maximum is also achieved.
- k_1, $k_2 \geq 1$ when V_m increases too much. The hysteresis loop is lost. This means that T is constant, whereas $\tau_{1,2}$ is modified.

To preserve the shape of the frequency-dependent pinched hysteresis loop in such a change, it is also necessary to change the values of the time constants in accordance with the applied frequency, taking into account that the numerical values of k_1, k_2 are kept within the interval $0 < k_1, k_2 < 1$ [7].

2.1 Effect of non-idealities and parasitic components on the values of obtained memductances

On the basis of obtained relations (8) and (9), normalised passive and active sensitivities of the memductances $W_1(\varphi_{12})$ and $W_2(\varphi_{12})$ are found as (see (15)) . In the derivation of (15), it is supposed that variation of supply V_{DD} and threshold voltage V_{Tn} can be neglected because of their stability and real (practically obtained) value of multiplication factors [(8) and (9)] with which the impact of these voltages on tracking error becomes less significant. On the basis of the above relations, we can conclude that the proposed emulator offers low passive and active sensitivities, lower than circuits described in [7] because there are fewer factors that condition sensitivity with factor 2.

If we take into consideration the influence of the parasitic components, i.e. the parasitic impedances, present at the input and output of VDTA (the non-ideal equivalent circuit of the VDTA is the same as Fig. 3 [7]), the passive components value of Fig. 1 can be modified as follows:

$$C_{eq} = C + C_{zc};\ R_{1eq} = R_1 \| R_p;\ R_{2eq} = R_2 \| R_z \| R_n$$
$$R_{eq1} = R_{eq} \| R_x;\ R_{eq2} = R_{eq} \| R_z \quad (16)$$

where the parasitic resistances R_p, R_n, R_z, R_{zc}, R_{x+} and R_{x-}, and the parasitic capacitances C_p, C_n, C_z, C_{zc}, C_{x+} and C_{x-} appearing in parallel at the corresponding terminals p, n, z, zc, $x+$ and x- (in ideal VDTA all of these parasitic resistances are approximately equal to infinity, while all parasitic capacitances are approximately equal to zero). Taking into account these parasitic elements, the value of obtained memductances can be rearranged as (see (17))

$$W_2 = \frac{K\beta_{mS}\beta_{mF} g_{mF} R_{eq2}}{(1 + R_{eq2} C_z s)}\left(\frac{\beta_{mF} g_{mF}}{C_{eq}}\Phi_{in} + V_{DD} - |V_{Tp}|\right) \cong K\beta_{mS}\beta_{mF} g_{mF} R_{eq2}\left(\frac{\beta_{mF} g_{mF}}{C_{eq}}\Phi_{in} + V_{DD} - |V_{Tp}|\right) \quad (18)$$

On the basis of the obtained relation, in order to preserve the performance of the proposed emulation circuits, the external capacitor C must be chosen in the way to satisfy $C \gg C_{zc}$. Owing to this setting, the parasitic capacitance effects can be absorbed in working frequencies. To reduce the impact of the parasitic resistances, the value of C must be chosen as $1/sC \ll R_{zc}$.

Monte Carlo analyses are used to investigate the effect of the process parameters and the mismatch between transistors [32]. As regards the mismatch between transistors and various process corners such as fast- and slow-mode operations for NMOS, PMOS transistors are taken into account to obtain the Monte Carlo analyses. This technique gives the lower and upper limits of the interval, which contains 95% of the error-absolute value of the difference between the memductances values obtained with (8) and (9) and (17) and (18). The conducted analysis in the SPICE program package is capable of statistically predicting the behaviour of the circuit in case of a deviation in the parameter values in the range of 5%, Fig. 4. The number of individual simulations was 2000. As shown in Fig. 4, the proposed floating memristor circuits show good performance at 2000 iterations, better than emulator circuit proposed in [7].

3 Simulation and experimental results

The proposed emulator circuits were verified using level-7 Taiwan semiconductor manufacturing company limited (TSMC) 0.18 μm CMOS process by SPICE simulation. Values for W and L, the channel width and length of transistors in the circuit in Fig. 2 are defined in the same way as in [7], while for MR_1 and MR_2 these were selected as $W/L = 60$ μm/2 μm. The power supply was ± 0.9 V, while the bias current was $I_{BF} = 160$ μA ($g_{mS} = 810$ μA/V). The control voltage V_C of the electronic resistor is selected as 0.65 V to obtain $R_{eq} = 1.47$ kΩ. In the course of the simulation, an input sinusoid voltage signal of varying frequency and amplitude $V_m =$ 200 mV was used, while the values of the resistors in the circuit in Fig. 1*a* was selected as $R_1 = 10$ kΩ and $R_2 = 1$ kΩ.

The voltage–current relationships of the proposed memductance emulators for various frequencies and different capacitor values are shown in Fig. 3 since memristors are also frequency-dependent elements. As shown in Figs. 3*a*–*c*, memristor behaves as non-linear and linear resistors when low and high frequencies are applied, respectively. It is clear that it is necessary to reduce the value of

$$-S_{R_1}^{W_1} = -S_C^{W_1, W_2} = S_K^{W_1, W_2} = S_{\beta_{mS}}^{W_1, W_2} = S_{R_{eq}}^{W_1, W_2} = S_{\varphi_{12}}^{W_1, W_2} = S_{R_2}^{W_1} = 1$$
$$S_{\beta_{mF}}^{W_1, W_2} = S_{g_{mF}}^{W_1, W_2} = 2 \quad (15)$$

$$W_1 = \frac{1 + R_{1eq} C_p s}{R_{1eq}}\left(1 \pm \frac{K\beta_{mS}\beta_{mF} g_{mF} R_{2eq} R_{eq1}}{(1 + R_{2eq} C_z s)(1 + R_{eq1} C_x s)}\left(\frac{\beta_{mF} g_{mF}}{C_{eq}}\Phi_{in} + V_{DD} - |V_{Tp}|\right)\right) \cong \frac{1}{R_{1eq}}\left(1 \pm K\beta_{mS}\beta_{mF} g_{mF} R_{2eq} R_{eq1}\left(\frac{\beta_{mF} g_{mF}}{C_{eq}}\Phi_{in} + V_{DD} - |V_{Tp}|\right)\right) \quad (17)$$

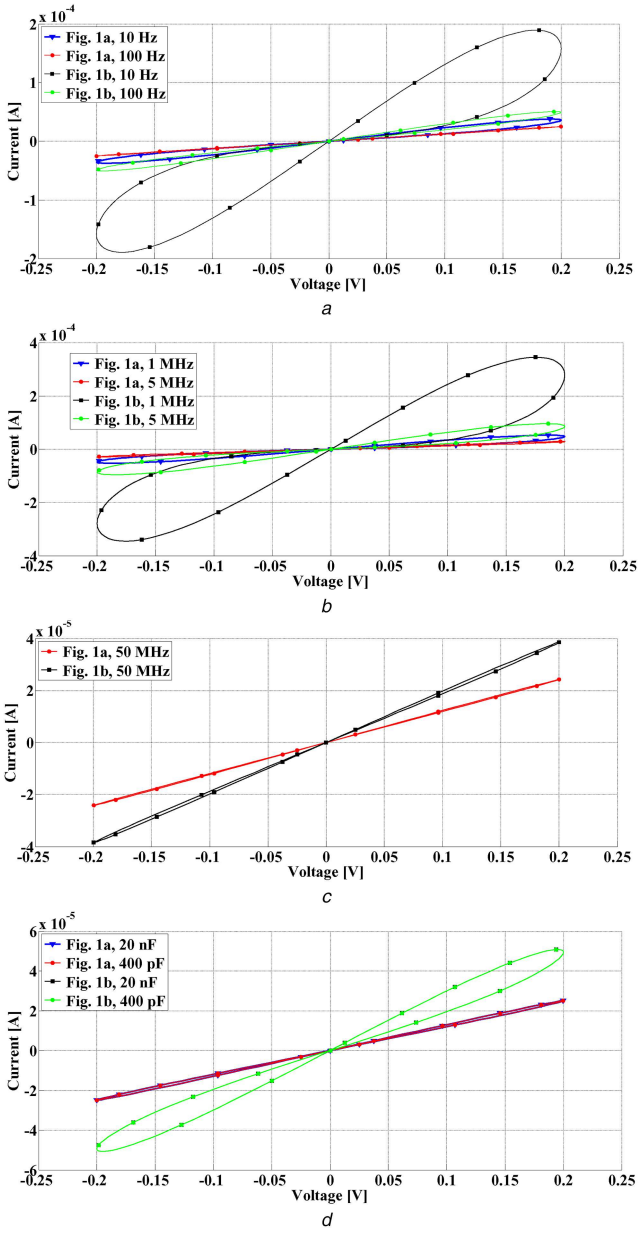

Fig. 3 *Simulation results*

(a) Pinched hysteresis loop of the proposed floating memristor emulators with the incremental property at different frequencies at 10 and 100 Hz and $C = 2$ μF, ***(b)*** Hysteresis loop at different frequencies at 1 and 5 MHz and $C = 10$ pF, ***(c)*** Hysteresis loop at frequencies of 50 MHz and $C = 10$ pF, ***(d)*** Comparison of hysteresis loop for ωC = constant at 10 and 500 kHz

capacitor C at higher operating frequencies in order to preserve the required shape character of the pinched hysteresis loop. Memristive behaviour has been obtained as expected.

Evaluation of the performances of the proposed emulation circuits was carried out at different frequencies, in a situation where the value of ωC is constant in Fig. 3*c*. From the obtained results, it can be seen that all the curves coincide because the values of k_1, k_2 remain unchanged in the situation when ωC is constant, thus confirming the theoretical analysis that is formulated through (11) and (12).

On the basis of derived relations (13) and (14), it can be concluded that by increasing the value of the capacitor, the lobe area of the pinched hysteresis loop is decreased as a result of the decrease in the values of the parameters k_1, k_2. This is also shown in Figs. 5*a* and *b*, where the simulation was performed for different capacitor values at a constant frequency.

To demonstrate the non-volatility and memductance change of the proposed memductance emulator, a non-volatility test [7, 13, 27] was performed, applying a pulse signal with a period of 1 ms, a pulse width of 0.2 ms and an amplitude of 100 mV to the proposed circuits in Fig. 1 ($C = 1$ nF). The time-domain simulation results for both the decremental memductance (Fig. 1*a*) and incremental memductance circuits (Fig. 1*b*) are given in Figs. 6*a* and *b*, respectively. From the presented results, it is concluded that the proposed emulator circuits possess the non-volatility character with respect to the fact that the same memductances' value can be observed when no pulse is present at the input [7, 17, 27].

Memristors are passive-circuit elements and cannot store energy. In other words, memristors have zero-phase difference between the voltage and the current. The transient characteristic of the proposed circuits in Fig. 1 is obtained with through a simulation test, in this case, a sinusoidal input signal for 10 kHz sinusoidal input voltage with 200 mV amplitude [7], while the corresponding passive components are chosen as $C = 1$ nF, $R_1 = 10$ kΩ and $R_2 = 1$ kΩ. As shown in Fig. 7, the phase of the current, which flows in memristor, is equal to the applied input voltage phase. Thus, the voltage–current curves show that memristor does not store energy, behaving rather as a passive-circuit element.

3.1 Experimental results

To provide experimental verification of the functionality of the proposed circuits for emulation in Fig. 1, two commercially available integrated circuits (ICs) MAX435 were used, as described in detail in [7]. During the experimental checks, the measured values of voltage and current using the TDS20114 oscilloscope (2500 samples) on the emulation circuits were first recorded and then transferred to the MATLAB environment, without altering to plot the curves [7].

The values of the passive components were selected in accordance with the values specified in the simulation procedure. Fig. 8 shows the results of comparison between simulation and experimental verifications of the circuits in Fig. 1.

Fig. 8 shows that the pinched hysteresis loop area decreases as the frequency increases, behaving as an inclined number '8' passing through the origin. This behaviours of the proposed circuits are determined not only by the ratio of the amplitude and frequency of the exciting voltage signal, but also by the value of the time constant of used emulators. Fig. 8 shows a high similarity between the simulation and experimental results. The results of the conducted experiments show that not only did the pinched hysteresis loop deviates from the origin in comparison with the simulation results, but also the surface of the loops in the first and third quadrants is not completely symmetrical and equal. The pronounced asymmetry and the offset result from the inherent non-idealities that occur in the process of making the input transistors of the ICs used, as the present parasitic components. By increasing the operating frequency, the size of the error can be reduced. Certainly, the size of the error deviation in relation to the simulation results is influenced by the mismatch in the biasing voltage [7]. The described non-idealities offset and asymmetry of transfer characteristics can limit the practical application of emulator circuits since the practically achieved output will slightly deviate from the desired. With the correct selection of components and proper biasing of used transistors, which will ensure the minimum mismatch in the transistors, and also by using additional calibration, the error in practical measurements can be reduced to an acceptable value.

For any practical use of the proposed floating memristor emulator, a careful adjustment of the involved components performed by using variable capacitors and resistors rather than fixed-value ones can compensate any possible inequalities and non-idealities, resulting in a floating memristor emulator with equal inflowing and output currents.

4 Conclusion

In this paper, two new flux-controlled floating memductance emulator circuits based on modified z-copy VDTA active-circuit element are proposed. The presented memristor circuits have been built with off-the-shelf solid-state components: two MAX435 ICs and one grounded capacitor, which is attractive from the point of

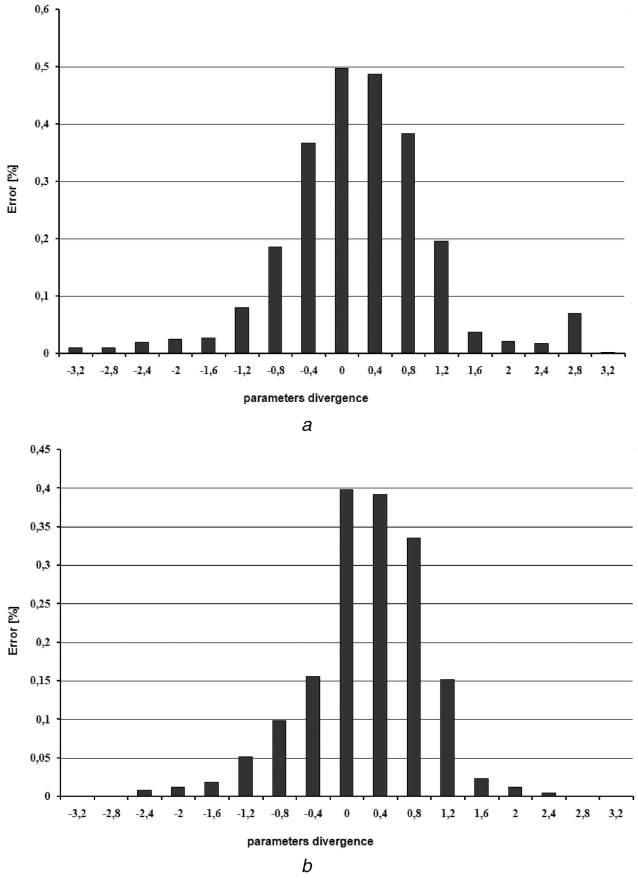

Fig. 4 *Distribution of errors, for divergence in the value of parameters, from their nominal values*

(a) Emulator circuits in Fig. 1*a*, ***(b)*** Emulator circuits in Fig. 1*b*

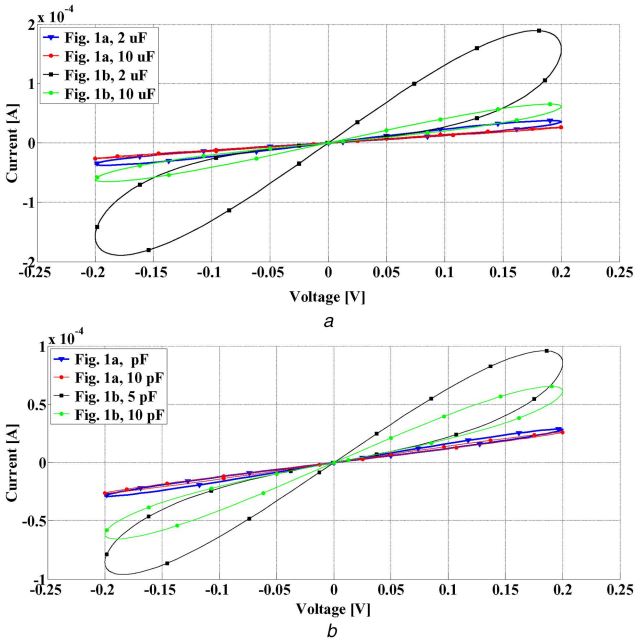

Fig. 5 *Simulation was performed for different capacitor values at a constant frequency*

(a) Comparison of the hysteresis loop for different capacitor values at 10 Hz, ***(b)*** Comparison of the hysteresis loop for different capacitor values at 10 MHz

view of the integrated circuit. The MOS capacitance can be used instead of the capacitor when memristors are operated in the high-frequency region [16]. Each feature of the proposed memristor emulators is tested via circuit measurements and simulations in SPICE software package-simulation results show that the maximum operating frequency for CMOS-based VDTA is 50

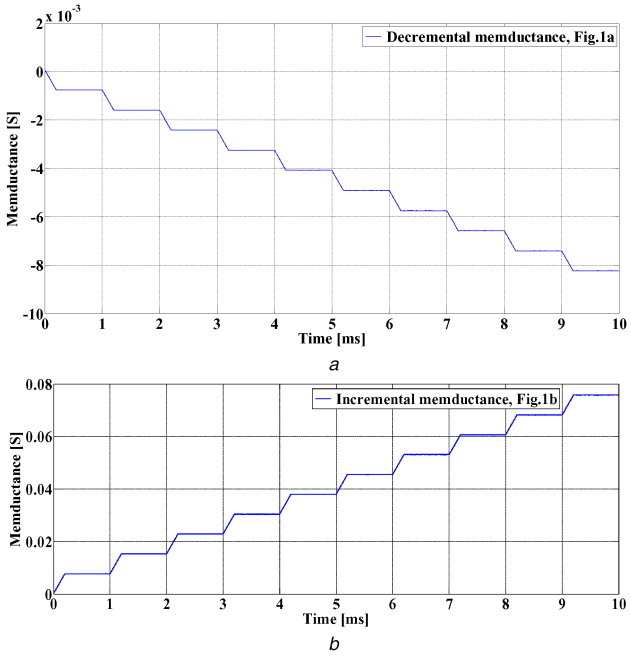

Fig. 6 *Time-domain simulation results for both the decremental memductance (Fig. 1a) and incremental memductance circuits (Fig. 1b)*

(a) Variation of memductance with time in the decremental configuration for circuits in Fig. 1*a*, ***(b)*** Variation of memductance with time in the incremental configuration for circuits in Fig. 1*b*

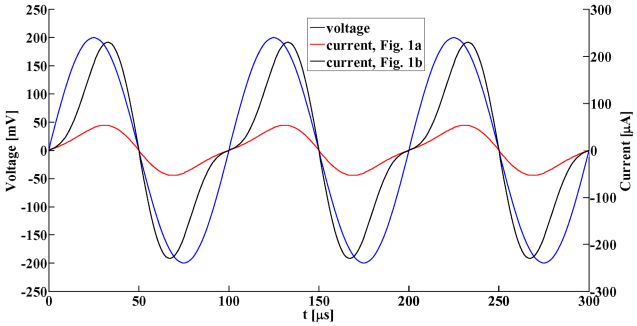

Fig. 7 *Time-domain response of the proposed memristors (f = 10 kHz)*

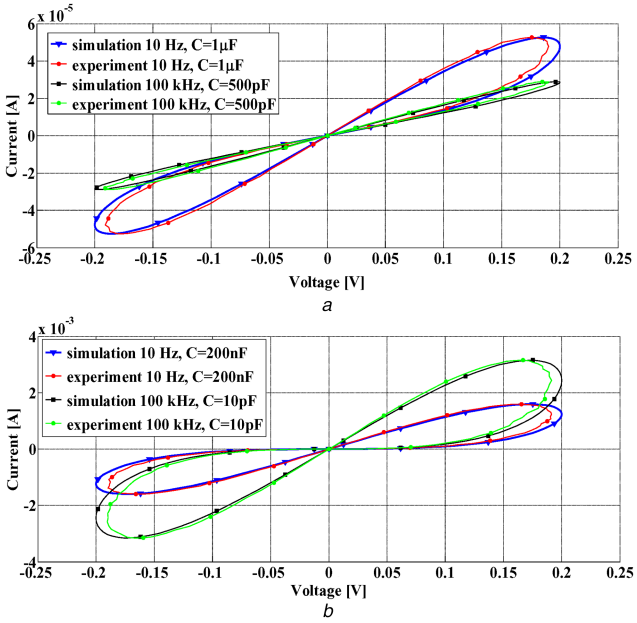

Fig. 8 *Comparison of pinched hysteresis loop at different frequencies and capacitor values*

(a) Emulator circuit in Fig. 1*a*, ***(b)*** Emulator circuit in Fig. 1*b*

MHz. The theoretical analyses, simulation and experimental results of memristor are obtained as expected and the results are compatible with both real memristors and previous studies. Compared to memristors emulators in the literature, proposed emulators contribute in terms of a number of active and passive elements, as well as operating frequency.

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