Received: 3 March 2021 | Revised: 3 September 2021 | Accepted: 29 November 2021

DOI: 10.1049/cds2.12106

IET Circuits, Devices & Systems

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH

New full-wave rectifier based on modified voltage differencing transconductance amplifier

Predrag B. Petrović

Technical Sciences Čačak, University of Kragujevac, Čačak, Serbia

Correspondence

Predrag B. Petrović, Technical Sciences Čačak, University of Kragujevac, Svetog Save 65, Čačak 32000, Serbia.
Email: predrag.petrovic@ftn.kg.ac.rs

Funding information

Ministarstvo Prosvete, Nauke i TehnoloÃ¡kog Razvoja, Grant/Award Numbers: 42009, 172057

Abstract

A full-wave rectifier based on a modified voltage differencing transconductance amplifier-MVDTA and four n-MOS transistors (or inverting full-wave rectifier), with no use of any passive elements is proposed in this paper. The proposed design is suitable for a low voltage and high frequency input voltage/current signal. The used MVDTA possesses certain new connections without any changes in the original circuit resources of VDTA. The proposed configuration possesses satisfactory zero crossing performance, excellent linearity, low component count—a simple and compact structure—which makes it an adequate candidate for implementation in the form of IC circuits. The amplitude-waveform of the current/voltage rectified signal at the output of the proposed circuit can be electronically controlled by the applied bias currents. The influence of possible non-ideality and parasitic effects was analysed, while the effects of the parasitic are only marginal due to the absence of any passive elements. To verify the validity of the presented circuits, SPICE simulations deploying 0.18 μm CMOS technology parameters and supply voltage of ±0.9 V are reported, fully consistent with the theoretical predictions. The noise and Monte Carlo analyses were also performed in order to obtain further insight into the robustness of the proposed design. The proposal is also supported by experimental results in order to confirm the workability of the proposed solution.

KEYWORDS

analogue integrated circuits, analogue processing circuits, current-mode circuits, MOSFET circuits, rectifying circuits

1 | INTRODUCTION

Rectification as one of the basic function-operations in signal processing is very intensively used in instrumentation, measurement, communication circuits and systems such as various nonlinear analogue signal-processors, peak-value detectors, ammeters, AC voltmeters and wattmeter's, RF demodulators, piecewise linear function generators, signal-polarity detectors and averaging circuits [1]. Such a wide and diverse application of high-performance rectifier circuits poses a need for the realisation of high quality and versatile precision rectifiers, which makes it one of the most current topics in the field of research and design of analogue signal processing circuits.

Several rectifier designs are reported in the literature based on various active blocks deploying voltage/current (VM/CM) mode [2–9] approach for the full-wave rectifier. This access overcomes the limitations posed by classical diode rectifiers and those based on the application of the operational amplifiers - OA. The threshold voltages of diodes introduce a great limitation in practical application of the diode-only rectifiers, while the already established OA-based rectifiers show restriction on the frequency range of operation due to the limited slew rate and gain-bandwidth product [2]. Some of the newly designed OAs possess a slew rate of 1.5kV/μs, and a gain-bandwidth of 4 GHz [10], but until now this type of OA has not been used for the realisation of full-wave rectifiers. In [2, 3] rectifiers are designed using a single EXCCII analogue building

block and extra n-MOS transistors, providing rectified outputs in dual phase simultaneously from the same topology [2]. Using voltage conveyors (VCs) as active blocks, a new versatile full wave rectifier circuit is described, providing the rectified output signal in both the form of voltage and current, while the input signal can also be applied as current or voltage based on the application [4]. The rectifier circuit [5] employs a dual-output second-generation current conveyor (DO-CCII) as the active block for realisation, while [6] uses the CFOA-current feedback operational amplifiers. A new current mode full wave rectifier formed by using PMOS and NMOS-based Low Voltage Cascode Current Mirror (LVCCM) was proposed in [7]. Rectifiers based on the use of current conveyors [8, 9] are capable of offering a wide bandwidth, large dynamic range, high slew rate and low consumption [8].

The paper proposes a new full-wave rectifier circuit, employing only one active element—an MVDTA and four MOS transistors. MVDTA is practically a variant of a well-known VDTA, first introduced in [11], with minor modifications in the internal structure of the active element itself, making it possible to perform processing in a new and effective way. The MVDTA as a platform offers numerous advantages over other active elements—a small number of transistors in the implementations, their easy pairing (MVDTA has a simple and symmetrical structure), controllability, and excellent impedance levels at the input and output allowing for easy connection both in the cascade and with other circuits, without special buffering. In addition, an extended frequency range is provided in relation to the hitherto known solutions, which are also based on the use of active elements of up to 50 MHz. The proposed circuit does not need to utilise special bias sources, and in this way, it is free of body effect for all transistors. The circuits use a single grounded electronic resistor, which benefits from the integrated circuit. No component matching is needed for their realisations. Use of the MVDTA leads to compact circuit structures, providing better linearity in the DC transfer characteristic within a wider voltage and current range in [8, 9]. In addition, the offered solution has a satisfactory zero crossing characteristic in a wide frequency range, without any major distortions in operating range and with a possibility of electronic tuning; the gain of transfer function provides an external parameter to control the rectified output of the proposed circuits without altering the other parameters of the design. According to the available literature, the circuit proposed here for full-wave rectification is the first of its kind that is based on the use of MVDTA or VDTA.

2 | PROPOSED CONFIGURATION OF RECTIFIER CIRCUITS

Figure 1a shows the proposed full-wave rectifier. It employs only one active component–MVDTA, and four extra n-MOS transistors.

The functional relations (current-voltage) between the various ports of MVDTA are given by Equation (1). [12]

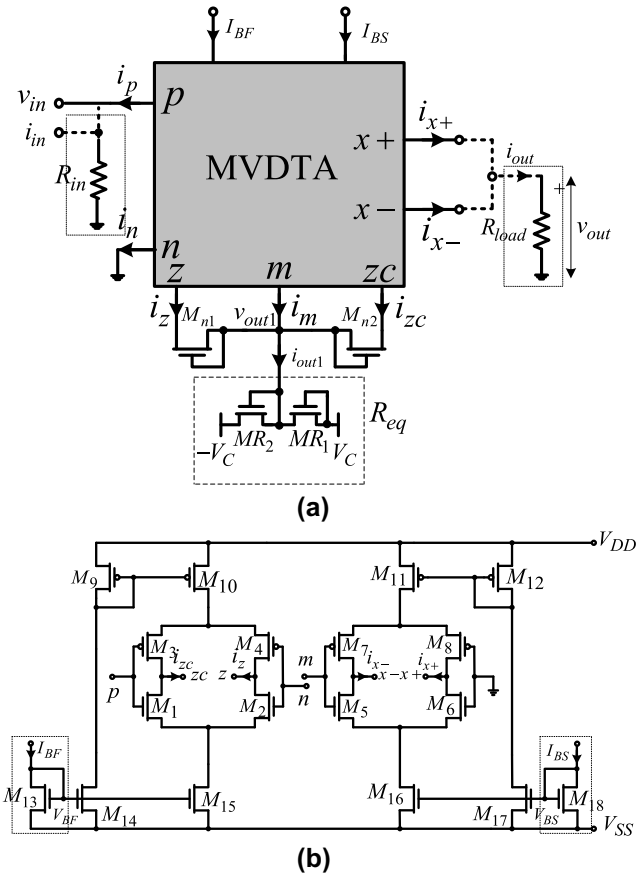

FIGURE 1 (a) Proposed full-wave rectifier, (b) CMOS implementation of MVDTA

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_{zc} \\ i_m \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 \\ -g_{mF} & g_{mF} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & g_{mS} \\ 0 & 0 & -g_{mS} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_m \end{bmatrix} \quad (1)$$

where, g_{mF} and g_{mS} are transconductance gains of MVDTA (two dependent transconductance gain stages). Its gains can be controlled electronically by biasing voltage or current, respectively [13]. A copy of the current i_z is available at the zc-terminal (i_{zc}); z and zc, that is the positive and negative outputs of the first OTA section are auxiliary high impedance ports [12].

Figure 1b shows the possible CMOS realisation of MVDTA (it is a seven-terminal block), in which the transconductance gains g_{mS} and g_{mS} can be varied electronically by currents I_{BF} and I_{BS}.

As we can see in Figure 1b, the MVDTA is composed of two Arbel-Goldminz transconductances [11], so that the values of g_{mF} and g_{mS} are determined by the output transistor transconductance, which can, respectively, be approximated as [12].

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1+g_2}\right) + \left(\frac{g_3 g_4}{g_3+g_4}\right); g_{mS} \cong \left(\frac{g_5 g_6}{g_5+g_6}\right) + \left(\frac{g_7 g_8}{g_7+g_8}\right) \tag{2}$$

$$g_i = \sqrt{\mu_i C_{ox} W_i I_{BF}(I_{BS})/L_i}, \quad i = 1, \ldots 8 \tag{3}$$

where μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of the ith MOS transistor, respectively. On the basis of such dependency -equation (2), it follows that temperature dependence of MVDTA is related to temperature dependence of g_m, depending upon the absolute magnitude of V_T (threshold voltage), whereas the approximate absolute change in V_T is −2.4 mV/°C. The temperature dependence of mobility is $\mu(T) = \mu(T_0)\ (T/T_0)^{-1/5}$. While the threshold voltage decreases with the temperature in the order of 0.24%, the mobility decreases with the temperature in the order of 1.5%. Obviously, the mobility decrease is dominant on the g_m decreases with the increasing temperature.

An electronically controllable resistor in Figure 1a -R_{eq}, can be adjusted through a control voltage V_C as $R_{eq} = (L/W)_{MR1,2}/(2\mu C_{ox}\ (V_C\text{-}V_{Tn}))$ (V_{Tn} is the threshold voltage of the NMOS transistor) [12]. We assume that MR_1 and MR_2 are matched and operate in saturation regions. By using the realised electronic regulated load on port m of the MVDTA in this way, the possible influence of the passive load on the realised transfer function of the proposed rectifier is reduced. The influence of parasitic effects—impedances on the operation of the circuit in Figure 1—is reduced. In addition, the possibility of an additional control of the magnitude of the rectified output voltage/current signal via the control voltage V_C is introduced.

The transistor M_{n1} (M_{n2}) is ON (OFF) for $v_{in} > 0$, and OFF (ON) for $v_{in} < 0$. This is indicated from the relations given in Equation (1). The voltage of the port m (Figure 1a) is then defined as

$$v_m = v_{out1} = \begin{cases} g_{mF} R_{eq} v_{in}; & v_{in}(t) \geq 0 \\ -g_{mF} R_{eq} v_{in}; & v_{in}(t) < 0 \end{cases} \Rightarrow v_{out1} = g_{mF} R_{eq} |v_{in}||_{VM}$$

$$i_{out1} = i_z + i_{zc} = g_{mF}|v_{in}| = g_{mF} R_{in} |i_{in}||_{CM} \tag{4}$$

while the current i_{out1} is a rectified waveform of the input voltage multiplied by the transconductance of the first stage of MVDTA, g_{mF}. CM denotes current- and VM voltage-mode of the operation. From Equation (4) we can conclude that v_{out1} is a full-wave rectified form of the input voltage signal (i_{out1} is a full-wave rectified version of the input current).

With the obtained value of the voltage v_m, we arouse the second stage of MVDTA, and based on Equation (1) (in ideal case) it follows that

$$i_{out} = \begin{cases} i_{x+} = g_{mF} g_{mS} R_{eq} |v_{in}(t)||_{TC} = g_{mF} g_{mS} R_{in} R_{eq} |i_{in}(t)||_{CM} \\ i_{x-} = -g_{mF} g_{mS} R_{eq} |v_{in}(t)||_{TC} = -g_{mF} g_{mS} R_{in} R_{eq} |i_{in}(t)||_{CM} \end{cases}$$

$$v_{out} = i_{out} R_{load} = \pm g_{mF} g_{mS} R_{load} R_{eq} |v_{in}(t)||_{VM}$$

$$v_{out} = \pm g_{mF} g_{mS} R_{in} R_{load} R_{eq} |i_{in}(t)||_{TI} \tag{5}$$

where TC denotes the transconductance-mode and TI the transimpendance-mode of operation . The circuit (Figure 1a) has two outputs: whereas one provides the noninverting full-wave rectifier function (output port $x+$), the other (output port $x-$) provides the inverting full-wave rectifier function.

It is completely clear (Equation (4)) that it is possible to use only the first stage of MVDTA for the realisation of a full-wave rectifier, but with the second stage (Figure 1b) a much greater flexibility in choosing the mode of operation is obtained, and it is possible to realise an inverting full-wave rectifier.

The transfer function of the rectifying circuit (Figure 1a) can be changed with the value of the variable MOS resistance R_{eq} - Equation (5) - and thus the amplitude of the rectified output voltage signal. The magnitude of the output current/voltage signal value can be additionally controlled by changing the value of the currents I_{BF} and I_{BS} (transconductance parameters of MVDTA). Since the rectifier function of the proposed circuit is realised without the use of a diode, it is also possible to process precisely the input low-amplitude sine wave signals, even at levels below the threshold voltage of the diode [8].

3 | NON-IDEAL AND PARASITIC ANALYSIS

In real practical conditions, the MVDTA possess non-ideal gains, tracking errors, for which reason the Equation (5) can be reformulated as

$$i_{out} = \begin{cases} i_{x+} = \beta_F \beta_S g_{mF} g_{mS} R_{eq} |v_{in}(t)| \\ i_{x-} = -\beta_F \beta_S g_{mF} g_{mS} R_{eq} |v_{in}(t)| \end{cases} \tag{6}$$

where β_F and β_S are defined as the tracking errors of the first and second stages of MVDTA, respectively. Typical values of these parameters (we can observe them as non-ideal transconductance gains of MVDTA stages) are in the range of 0.9–1, with an ideal value of one. Generally, these tracking factors remain constant and frequency-independent within low to medium frequency ranges [8]. From the above Equation (6), we can conclude that the proposed full-wave rectifier exhibits the magnitudes of all the sensitivity values; normalised passive and active sensitivities are equal to or less than unity in magnitude and the proposed circuits offer low passive and active sensitivities.

The transconductances g_{mF} and g_{mS} of MVDTA are frequency-dependent parameter-determining factors and their bandwidth limitation can be described by a single pole model, as follows

$$g_{mF} = \frac{g_{mF0}}{1 + s\tau_F};\ g_{mS} = \frac{g_{mS0}}{1 + s\tau_S} \tag{7}$$

where g_{mF0} and g_{mS0} are the transconductance gains at zero (low) frequency, while $\omega_F = 1/\tau_F$ and $\omega_S = 1/\tau_S$ are the corresponding pole frequencies. Here, τ_F and τ_S are delays corresponding to pole frequencies, respectively. In general, the values of these poles will depend on practical implementation of the MVDTA. Combining Equation (6) with Equation (7), the frequency-dependent output currents of the full-wave rectifier circuits in Figure 1 can be defined (re-written), respectively, as follows

$$i_{out} = \begin{cases} i_{x+} = \beta_F \beta_S g_{mF0} g_{mS0} R_{eq} \dfrac{\omega_F \omega_S}{(s + \omega_F)(s + \omega_S)} |v_{in}(t)| \\ i_{x-} = -\beta_F \beta_S g_{mF0} g_{mS0} R_{eq} \dfrac{\omega_F \omega_S}{(s + \omega_F)(s + \omega_S)} |v_{in}(t)| \end{cases} \tag{8}$$

Equation (8) indicates that the useful operating frequency range of the rectifier in Figure 1a can, respectively, be defined as $\omega << \min(\omega_F, \omega_S)$. The bandwidth of MVDTA can be improved by inserting a compensation resistor R at port p, and one voltage buffer realised with a pair of MOS transistors in the VDTA CMOS structure shown in [14]. The transconductance gain g_{mF} for this modified VDTA can be given as

$$g_{mF} = \frac{g_{mF0}}{1 + g_{mF0} R} \tag{9}$$

From Equation (9) it is clear that g_{mF} can be changed by resistance R, and in this way, the bandwidth of MVDTA can be changed as well, since it depends on g_{mF}.

The parasitic resistances R_p, R_n, R_z, R_{zc}, R_m, R_{x+} and R_{x-}, and the parasitic capacitances C_p, C_n, C_z, C_{zc}, C_m, C_{x+} and C_x [15] appear in parallel at the corresponding terminals p, n, z, zc, m, $x+$ and $x-$ (in ideal MVDTA all the parasitic resistances are approximately equal to infinity, while all parasitic capacitances are approximately equal to zero) [12].

If we take into consideration the influence of the parasitic components defined above (existence of parasitic port impendences), we come to a position where it is possible to analyse the operation of the proposed full-wave rectifier in a situation when it operates in a high frequency environment. We can conclude that

$$R_{mz} = R_m \| R_z; R_{mzc} = R_m \| R_{zc}; C_{mz} = C_m + C_z; C_{mzc} = C_m + C_{zc}$$

$$v_z = v_{out1} = \begin{cases} g_{mF} R_{eq} \left\| R_{mz} \right\| \dfrac{1}{sC_{mz}} v_{in} = g_{mF} \dfrac{R_{eq} R_{mz}}{R_{eq} + R_z + sR_{eq} R_{mz} C_{mz}} v_{in};\ \ v_{in}(t) \geq 0 \\ -g_{mF} R_{eq} \left\| R_{mzc} \right\| \dfrac{1}{sC_{mzc}} v_{in} = -g_{mF} \dfrac{R_{eq} R_{mzc}}{R_{eq} + R_{mzc} + sR_{eq} R_{mzc} C_{mzc}} v_{in};\ \ v_{in}(t) < 0 \end{cases} \tag{10}$$

$$i_{out} = \pm g_{mS} g_{mF} \frac{R_{eq} R_{mz(mzc)}}{R_{eq} + R_{mz(mzc)} + sR_{eq} R_{mz(mzc)} C_{mz(mzc)}} |v_{in}(t)|$$

$$v_{out} = i_{out} \frac{R_{load} R_{x+(x-)}}{R_{load} + R_{x+(x-)} + sR_{load} R_{x+(x-)} C_{x+(x-)}} \tag{11}$$

The following constraints must be overcome on the basis of the above equation [8]. The following must be satisfied for a proper operation of the proposed full-wave rectifier

$$\frac{R_{mz(mzc)}}{1 + \omega R_{mz(mzc)} C_{mz(mzc)}} >> R_{eq};\ \frac{R_{x+(x-)}}{1 + \omega R_{x+(x-)} C_{x+(x-)}} >> R_{load}$$

$$\omega \frac{R_{eq} R_{mz(mzc)} C_{mz(mzc)}}{R_{eq} + R_{mz(mzc)}} << 1;\ \ \omega \frac{R_{load} R_{x+(x-)} C_{x+(x-)}}{R_{load} + R_{x+(x-)}} << 1 \tag{12}$$

where $\omega = 2\pi f$ is the angular frequency and f is the operating frequency (frequency of the processed input signal). The useful frequency range is evaluated as follows

$$f \leq \min\left(\frac{0.1}{2\pi} \left(\frac{R_{eq} + R_{mz(mzc)}}{R_{eq} R_{mz(zc)} C_{mz(mzc)}} \right), \frac{0.1}{2\pi} \left(\frac{R_{load} + R_{x+(x-)}}{R_{load} R_{x+(x-)} C_{x+(x-)}} \right) \right) \tag{13}$$

In relation to Equation (13), we use $\leq$ instead of $<<$ (Equation (12)), because the maximal operating frequency f is defined as a 10th part of the angular frequency ω.

4 | SIMULATION AND EXPERIMENTAL RESULTS

The full-wave rectifier circuits proposed in Figure 1a were verified using a simulation procedure in the SPICE environment, with level-49 TSMC 0.18 μm CMOS process parameters. The aspect ratios of the MOS transistors in Figure 1b were taken as 16.1/0.7 for M_1, M_2, M_5, M_6; 3.6/0.36 for M_3, M_4, M_7, M_8, M_{13}, M_{18}; 16.64/0.36 for M_9–M_{12}; 4.5/0.36 for M_{14}–M_{17}; 0.8/0.18 for M_{n1} and M_{n2}, while for MR_1 and MR_2 these were selected as W/L = 60 μm/2 μm. For example, if the control

voltage V_C of the electronic resistor was selected as 0.65 V, we obtain R_{eq} = 1.47 kΩ. The power supply was ±0.9 V. Important DC and AC parameters of the proposed MVDTA circuits (Figure 1b) are summarised in Table 1 (with obtained values of port parasitic impedances), while the DC and AC transfer characteristics are shown in Figure 2. The min/max

TABLE 1 DC and AC parameters of MVDTA for two particular values of bias-control current

Parameter	Value for $I_{BF} = I_{BS}$ = 10 μA	Value for $I_{BF} = I_{BS}$ = 100 μA
p, *n* and *m* dc resistance, $R_p = R_n = R_m$	>1 GΩ	>1 GΩ
z output dc resistance R_z	446 kΩ	368 kΩ
zc output dc resistance R_{zc}	229 kΩ	229 kΩ
x+ and *x*- output dc resistance, $R_{x+} = R_{x-}$	1.33 MΩ	462 kΩ
p, *n* and *m* input capacitance $C_p = C_n = C_m$	11 fF	11 fF
x+ and *x*- output capacitance $C_{x+} = C_{x-}$	16 fF	16 fF
z output capacitance C_z	26 fF	26 fF
zc output capacitance C_{zc}	25 fF	25 fF
3dB attenauation for transfer from *p* input to *z* output K_{-3dB} ($p \rightarrow z$)	>1 GHz	>1 GHz
3dB attenauation for transfer from *p* input to *zc* output K_{-3dB} ($p \rightarrow zc$)	550 MHz	285 MHz
Transconductance of the first and second OTA, $g_{mF} = g_{mS}$	270 μS	512 μS
Corner frequency ω_F, ω_S	5.6 rad/s	7.3 rad/s

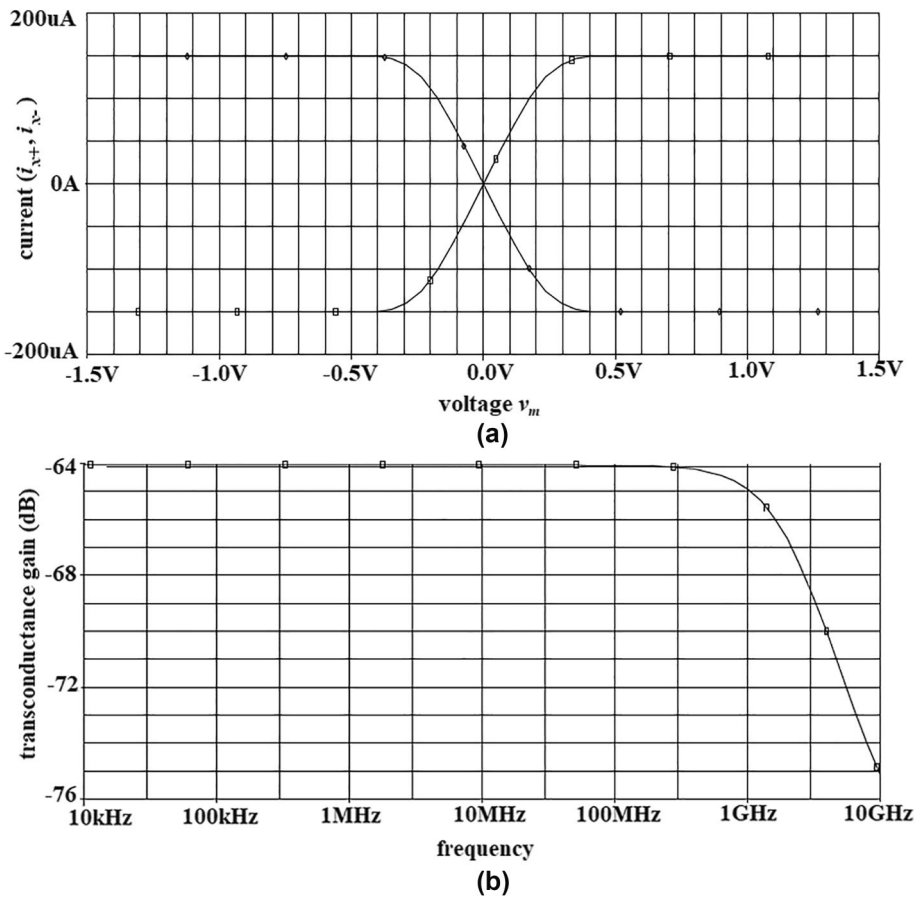

FIGURE 2 (a) DC characteristics of MVDTA, (b) AC characteristics of MVDTA (for $I_{BF} = I_{BS}$ = 100 μA)

value of the bias current is 5/300 μA—in this range MVDTA retains the characteristics defined here. DC characteristics are a plot showing the variation of i_{x+} and i_{x-} with respect to v_m. The AC characteristics show the variation of the transconductance gain g_{mF} with respect to the frequency. The simulation results show that the transconductance gain drops by 3 db at 2.163 GHz.

It is obvious from the data listed in Table 1 that the adjustment of $g_m(I_B)$ has a significant impact on the obtained parameters. The maximum power consumptions of the simulation circuits are 0.84 mW at ±0.9 V supply voltages.

The transient response of the proposed full-wave rectifier circuit is shown in Figure 3; considering the variable magnitude and frequency of the applied input voltage signal, the circuit operates in the transconductance mode. In Figure 3b, we can see how the proposed configuration works as the inverting full-wave rectifier (the output current was obtained from port i_{x-} of MVDTA). By changing the values of biasing currents (I_{BF} and I_{BS}), we demonstrate the tunability of the proposed circuits. The amplitudes of the output currents were changed in this way. From the enclosed figures, it is evident that a marginal delay occurs at a frequency of 40 MHz; this may be due to the internal parasitic components of the circuit.

The distortion at zero crossing, owing to the maximum slew-rate of the output current/voltage for the active device and turn-on and turn-off transition of MOSFETs, directly defines the highest applicable operating frequency limitation of the proposed rectifiers.

Figure 4 shows DC transfer characteristics of the proposed full-wave rectifier circuit for all operating modes (for $I_{BF} = I_{BS} = 10$ μA). The maximum input voltage signal amplitude obtained is approximately 350 mV. In Figure 4, the offset at zero crossing (worst case) is determined as 0.54 μA. Based on the presented results, it can be concluded that the proposed rectifier circuit shows

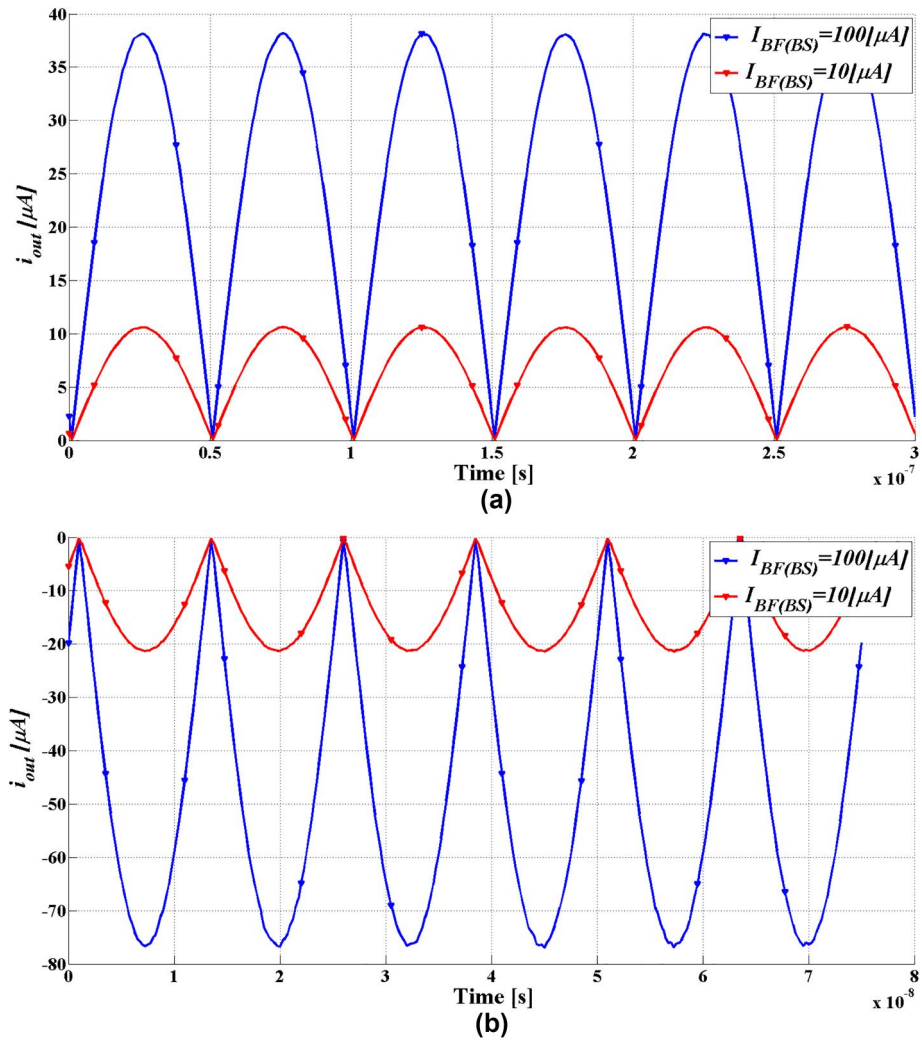

FIGURE 3 (a) Transient response at frequency f = 10 MHz and input amplitude of 100 mV (b) Transient response at frequency f = 40 MHz and input amplitude of 200 mV

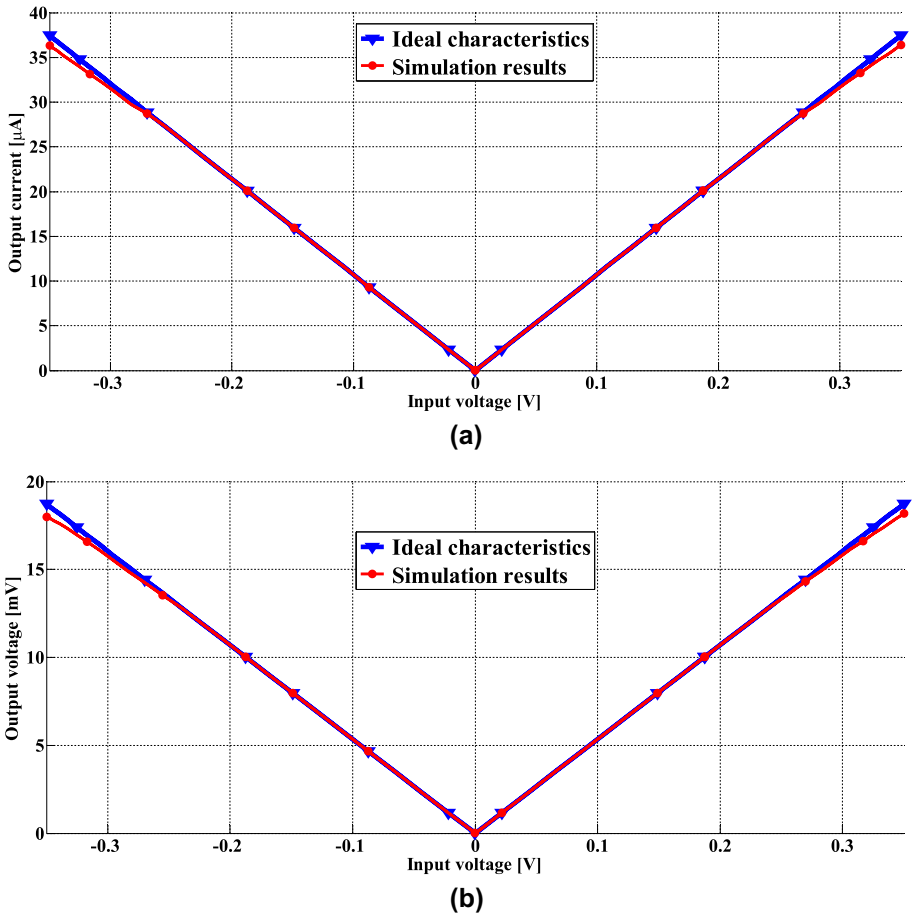

FIGURE 4 DC transfer characteristics of the proposed precision rectifier (a) Transconductance mode (b) Voltage mode for R_{load} = 500 Ω (c) Current mode for R_{in} = 35 Ω (d) Transimpendance mode, for R_{in} = 35 Ω and R_{load} = 500 Ω (e) DC transfer characteristics from the voltage input to v_m-$v_m(v_{in})$

a high degree of linearity, as well as a practically equal swing both for the positive and the negative variations of the signal amplitude, with the low-scale distortion occurring at the zero crossing [16]. The maximal relative error in relation to the ideal characteristics is 2% in the corner areas of the transfer characteristics. Figure 5 shows transient responses at the maximum input amplitude and the operation frequency of the proposed rectifier in VM and CM. In VM (Figure 5a), the input voltage amplitude was 350mV, while in CM (Figure 5b), the input current amplitude was 10 mA. In both modes of operation the frequency of the input signals was set as 50 MHz (I_{BF} = I_{BS} = 10 μA).

The AC transfer characteristics of the proposed circuit for all operating modes are shown in Figure 6a for the same parameter values as in the case of determining the DC characteristics. The former acknowledges a good working bandwidth of 50 MHz, whereas the latter shows a good linearity [4]. The important performance parameter of the rectifier circuit is the DC value transfer (ρ_{DC}) [4, 17, 18]—the purity of rectified output voltage and current signals is evaluated as the ratio of simulated DC values to the ideal DC values, as a function of the magnitude and frequency. The ideal value of this ratio, which is shown by ρ_{DC}, is unity. The simulation results of ρ_{DC} versus frequency of the full-wave rectifier within the range 1—100 MHz and corresponding magnitudes of the input voltage/current signals have been shown in Figure 6b. By increasing the frequency and decreasing the magnitude of the input signal, the deflection from the ideal operation is indicated by a change, mostly a decrease in ρ_{DC} below one. Figure 6b shows the simulation results of ρ_{DC}. It is evident that ρ_{DC} values are close to the ideal unity, which confirms the accurate feature of the rectifier.

The variable temperature environment from 25°C to 75°C is considered to show the robustness of the presented design ($I_{BF} = I_{BS} = 100$ μA). Based on the obtained results in Figure 7, it can be noticed that only very little deviation occurs in the response as a result of the change in the environment temperature—the rectified signal amplitude shows a minute deviation with temperature. It should be noted that such results were obtained without an additional circuit that could perform

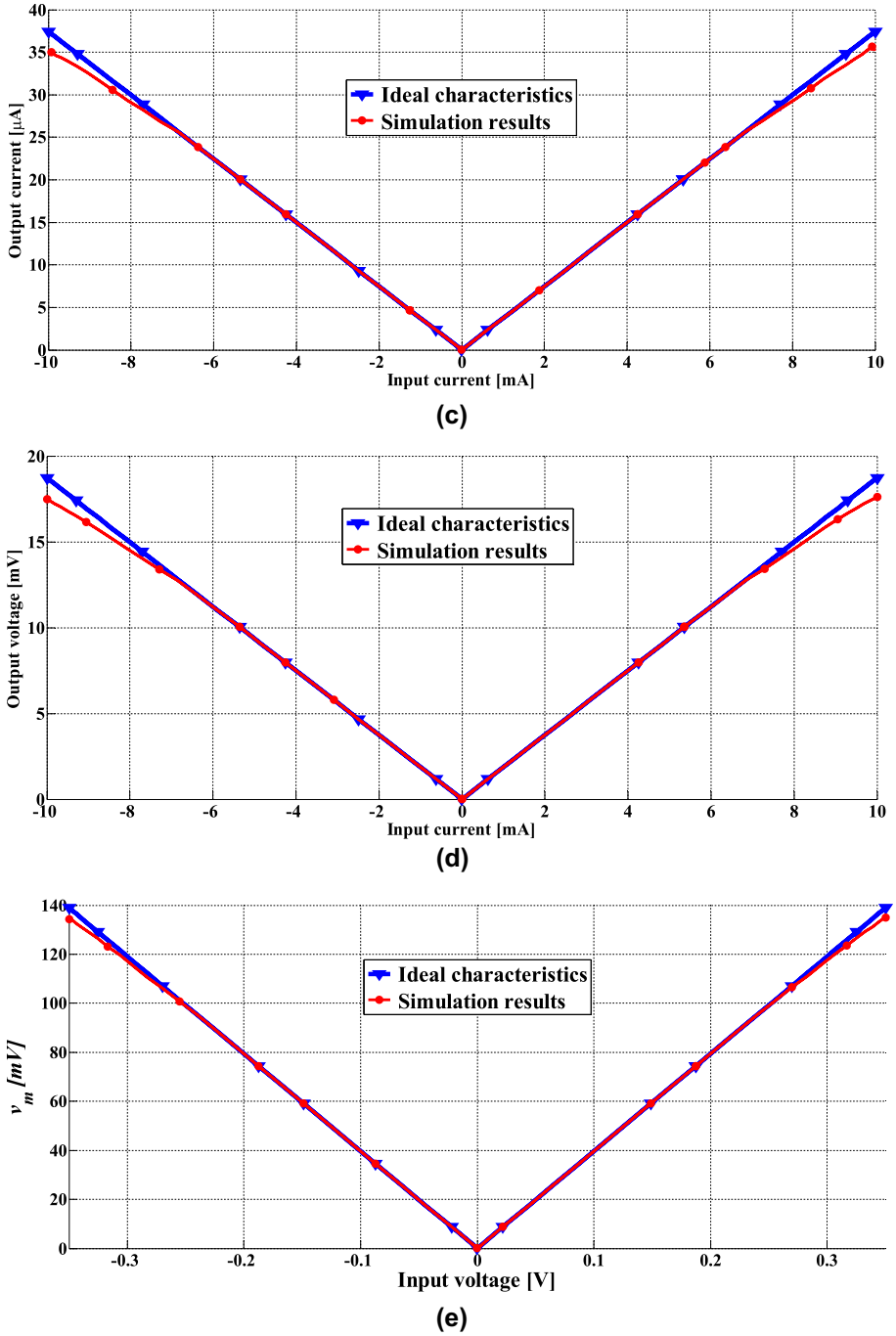

FIGURE 4 (Continued)

temperature compensation. It is concluded that with increasing temperature there is only a small decrease in the amplitude of the rectified output signal. The obtained results correspond to the theoretical discussion and values of temperature dependence of V_T and mobility as described in Section 2 of the paper. An input voltage signal at the frequency of 10 MHz was used during simulation tests conducted in this manner [16].

It is well known that the Monte Carlo analysis (the performance study) offers a unique tool to study and analyse the robustness as well as the uncertainty of the proposed realisation of the full-wave rectifier circuit for transistor mismatch [19]. For the input voltage signal of amplitude 200 mV and frequency 20 MHz ($I_{BF} = I_{BS} = 10$ μA), Monte Carlo simulation is performed 500 times, with 5% Gauss deviation of gate oxide thickness (t_{ox}) and relevant transistors' width and length (of all the MOS transistors) and 10% Gauss deviation of V_{TH0} (threshold voltage) are achieved as in Figure 8a. The DC Monte Carlo analysis is shown in

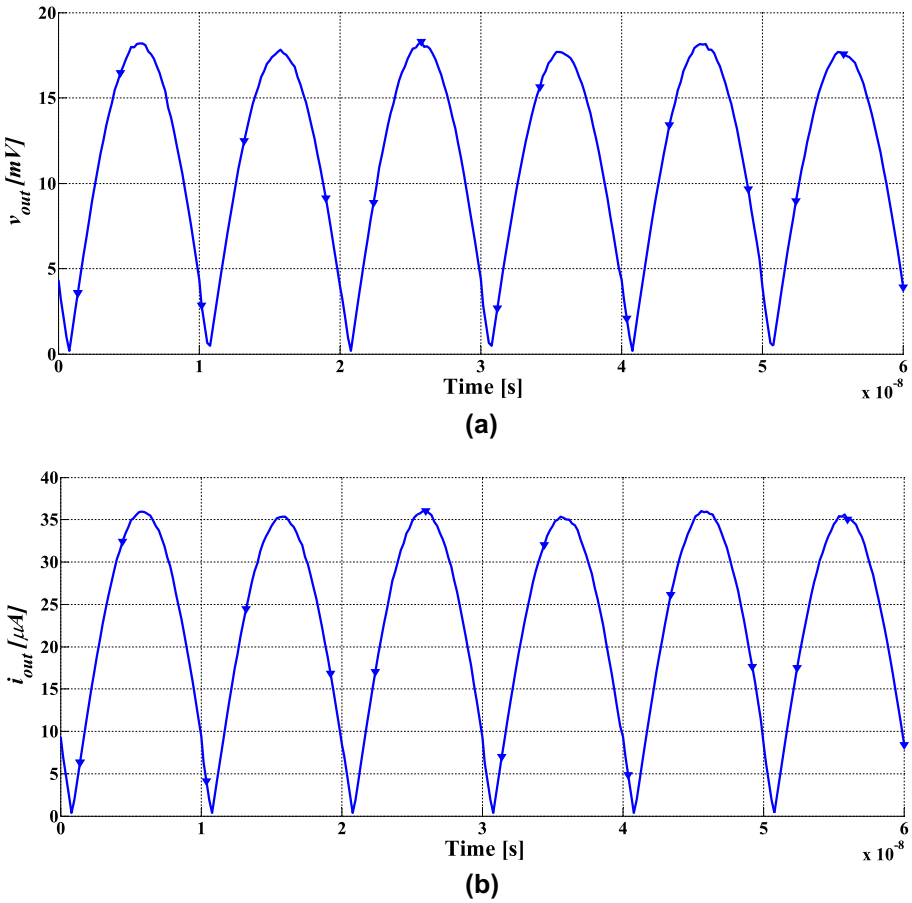

FIGURE 5 (a) Transient response in VM for R_{load} = 500 Ω and input amplitude of 350 mV (b) Transient response in CM for R_{in} = 35 Ω and input amplitude of 10 mA

Figure 8b. It is seen that the rectifier circuit is still operational within acceptable limits despite having a slight deviation in the output response.

Process corners like Typical NMOS Typical PMOS (TT), Fast NMOS Fast PMOS (FF), Slow NMOS Slow PMOS (SS), Fast NMOS Slow PMOS (FS), and Slow NMOS Fast PMOS (SF) variations are analysed in Figure 8c. There are slight amplitude changes in corner analysis, but the proposed rectifier circuit has still exhibited satisfactory operation performance in the whole design space of process corner variations. In summary, the proposed circuit can be operated successfully in wide temperature ranges and different radical conditions. The histogram in Figure 8d shows the distribution of the ρ_{DC} of the rectifier determined based on Monte Carlo process/mismatch analysis (200 runs). The input voltage was set to 200mV/20 MHz. The mean value of ρ_{DC} is 0.984 and the standard deviation is around 5.6 m, which shows tolerable circuit sensitivity to transistor mismatches. An additional assessment of the effectiveness of the proposed solution can be performed based on the methodology proposed in [20], according to which the yield of such two-stage OTA (proposed MVDTA) can be estimated beyond 95%. In [20], the analysis of the two-stage OTA was performed, with about the same number of transistors as MVDTA. It was shown that, based on the proposed approach and the results of HSPICE simulation, in later practical implementation and production of such full-wave rectifiers, the computation cost can be reduced by 20 times for an error less than 8%.

The output noise behaviours of the proposed rectifiers in correlation to frequency have also been simulated [21]. For the current-, voltage-, transimpedance- and transconductance-mode rectifiers, the equivalent output noises at an operating frequency of 50 MHz are found to be 4.8 nA/$\sqrt{\text{Hz}}$, 6.9nV/$\sqrt{\text{Hz}}$, 13.4nV/$\sqrt{\text{Hz}}$, and 14.2 nA/$\sqrt{\text{Hz}}$, respectively.

4.1 | Experimental results

In order to carry out the experimental verification of the proposed concept-circuit for rectification of either the voltage or the current input signal, since MVDTA is not a

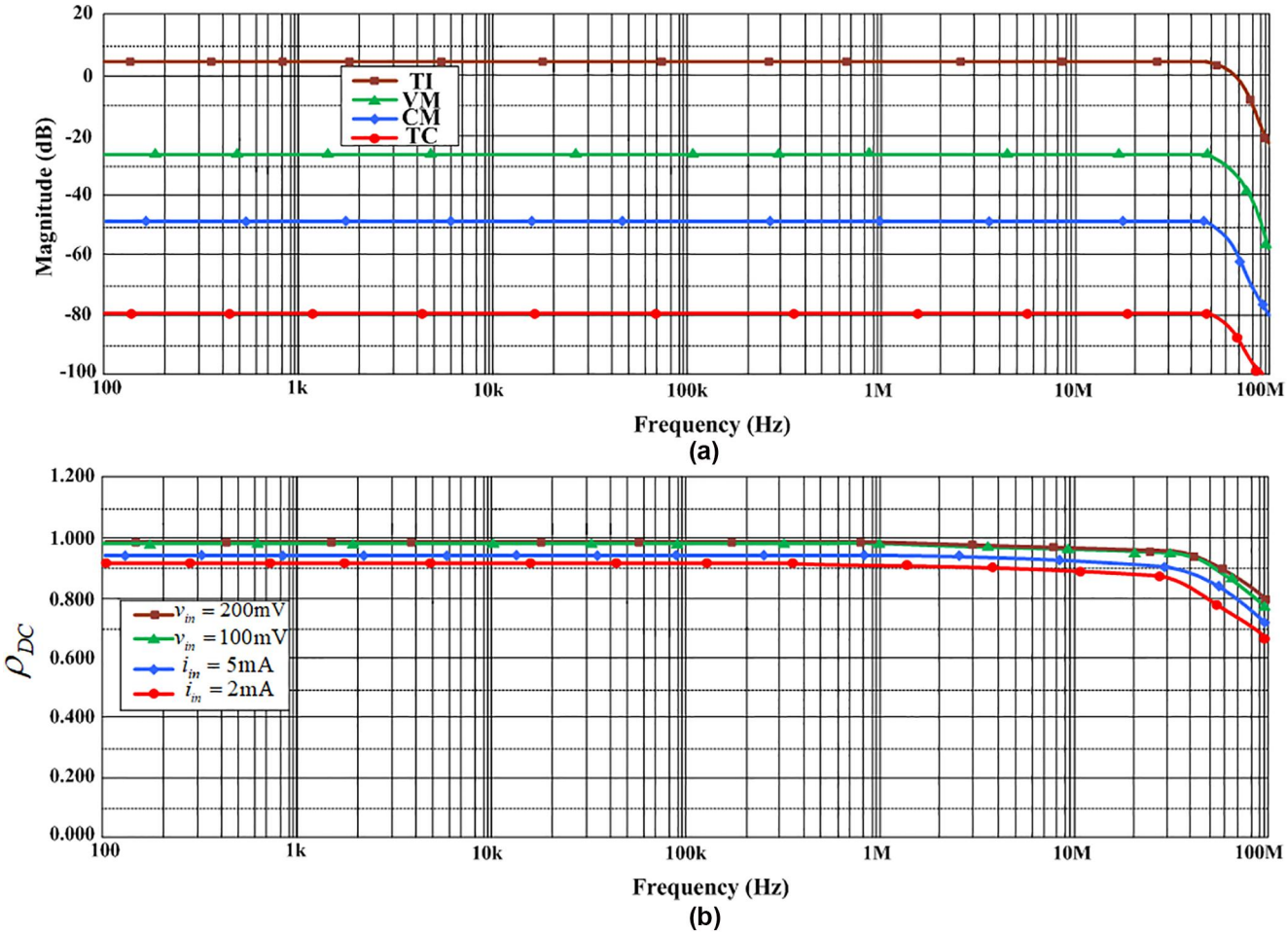

FIGURE 6 (a) AC transfer characteristics (b) DC transfer ratio versus frequency with various magnitudes for I_{DCsim}/I_{DCth} and V_{DCsim}/V_{DCth}

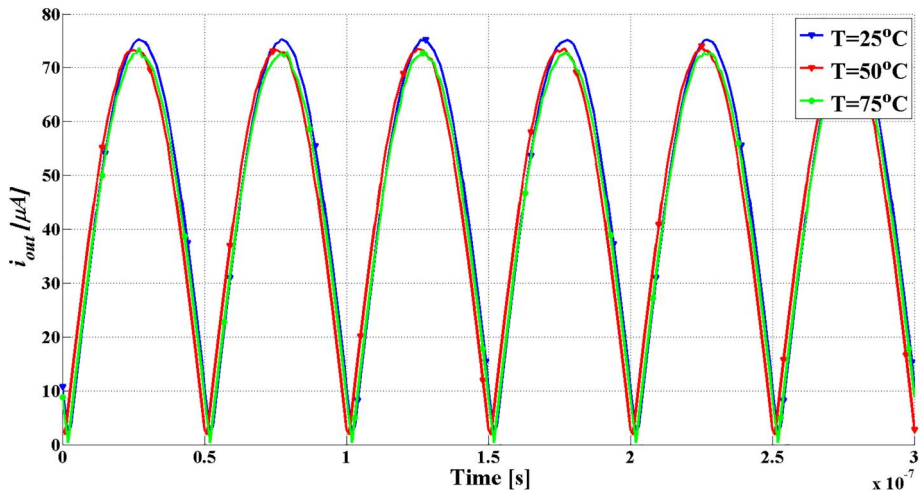

FIGURE 7 Temperature analysis of the proposed rectifier circuit—response in different temperature conditions—for the input voltage signal of amplitude

commercially available component, the circuit shown in Figure 1 was built with off-the-shelf electronic devices. The MVDTA is implemented as shown in Figure 9a using ICs MAX435 by Maxim Integrated [12, 22] (e.g., the VDTA can be realised by utilising a single LM13700 integrated circuit [23]). The DC power supply voltages were equal to ±5V.

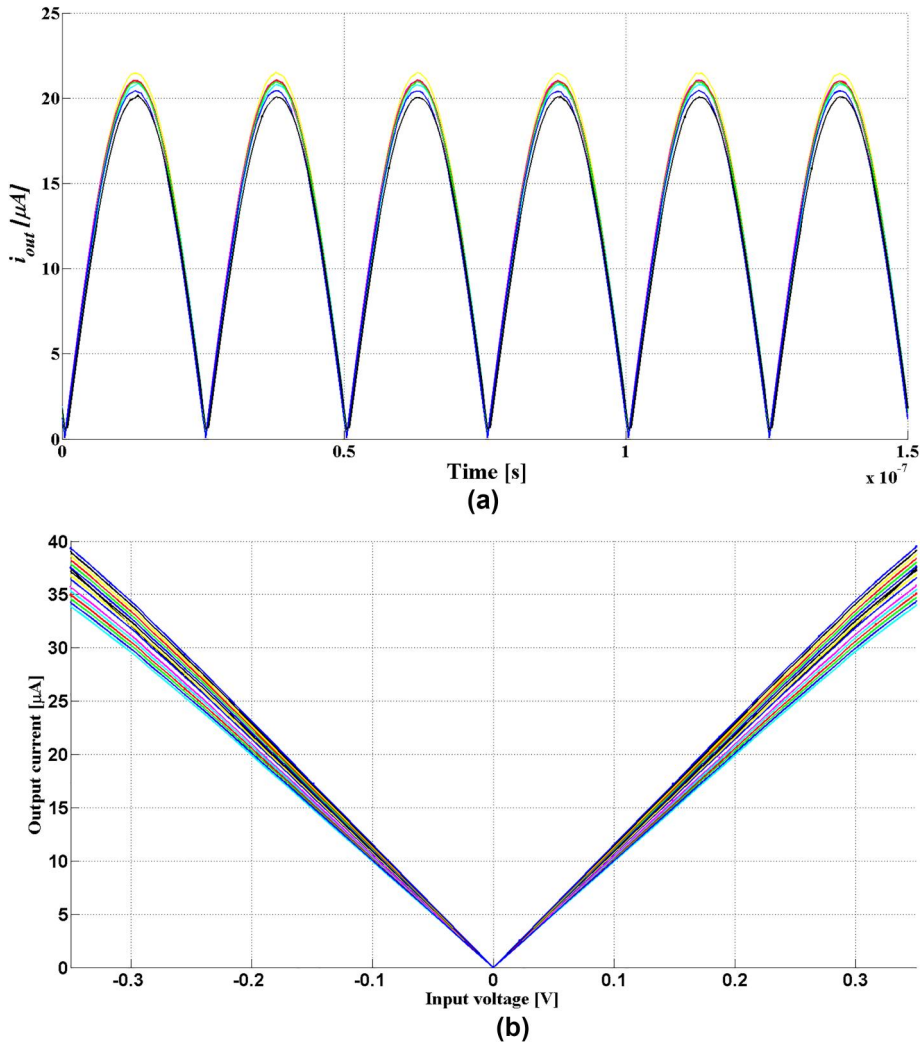

FIGURE 8 Monte Carlo analysis of the presented rectifier circuit (a) Time response (b) Input-output DC characteristics (c) Process corner analysis (d) Histogram of the ρ_{DC} based on Monte Carlo analysis for 200 runs

The R_{eq} was replaced with the resistance of 100 Ω, while two IRF540 N were used instead of the transistors M_{n1} and M_{n2} (Figure 1). The tranconductance gains for CMOS-based MVDTA, defined in Equations (2), are not the same as for MAX435, which is used for practical implementation of the MVDTA. It is completely clear that the results obtained in this way are worse than the simulation ones due to the generated imperfections that are a consequence of such a discrete realisation. Experimental verification conducted in this way only confirms the correctness of the proposed processing concept based on the use of an active element such as MVDTA, with clear guidelines on the possible performances achieved by the simulation and obtained results after performing a Monte Carlo analysis. For experimental measurements, the data is recorded by the oscilloscope TDS20114 (3000 samples), and then transferred into the MATLAB environment, without altering to plot the curves [12].

Figure 9b shows the results of the measurements on the experimental setup, described above, for the amplitude of the input voltage signal of 500 mV. The experiment is performed at a frequency of 500 kHz. It can be noted that the amplitude of the output current waveform shows a minute offset due to the tracking errors, parasitic components, and mismatching in the transistors. In addition, the experimental setup has frequency limitations; the operating bandwidth is around 10 MHz since these commercial ICs have frequency limitations and parasitic effects due to interconnections.

4.2 | Comparison

The performance of the presented full-wave rectifier circuit is compared with the available literature as shown in Table 2. It can be observed from Table 2 that the

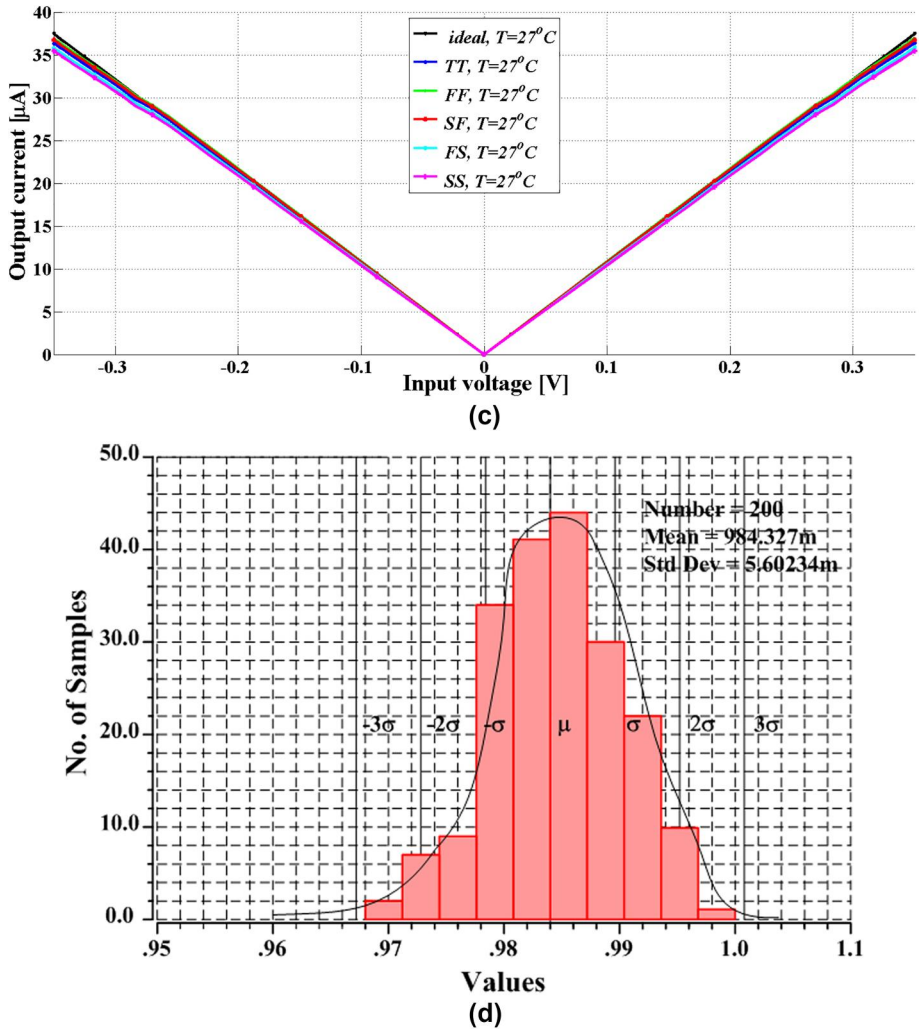

FIGURE 8 (Continued)

presented design of the full-wave rectifier circuit does not require any passive components and provides electronic tunability features. In addition, it employs only one type of active element— the MVDTA—which is cascadable and does not need any auxiliary current buffer and voltage buffer as circuits described in [4]. In order to use the proposed circuit with current input or voltage output, the impedances of the floors to which this circuit is connected must be suitable for this situation. It possesses an extended frequency range in relation to the known solutions, which are also based on the use of other types of active elements. Based on the obtained and proved performances, the proposed full-wave rectifier can be implemented in many areas [8] as follows: signal processing, realisation of the current mode filters, amplifiers, radio frequency oscillators, conditioning and instrumentation of low-level signal and DC converters, oscillators and low noise amplifiers, and ASK/FSK modulators.

5 | CONCLUSION

The paper presents a new precise full-wave rectifier structure employing only one MVDTA as an active element and four NMOS transistors. All the stated theoretical assumptions that support the described design have been fully confirmed through SPICE simulations using 0.18 μm CMOS technology parameters and experimental measurements. The obtained DC and AC characteristics of the full-wave rectifier show good linearity in the wide voltage/current range. Taking into account deviations of process parameters and dimensions of MOS transistors, performances of the proposed rectifier also have been investigated by the Monte Carlo and process corners analysis. The proposed rectifier can very successfully operate at high frequency, up to 50 MHz, featuring good zero crossing performance and low component count, so that it is appropriate for IC implementation. In addition to all of the above, the proposed circuit has good temperature stability

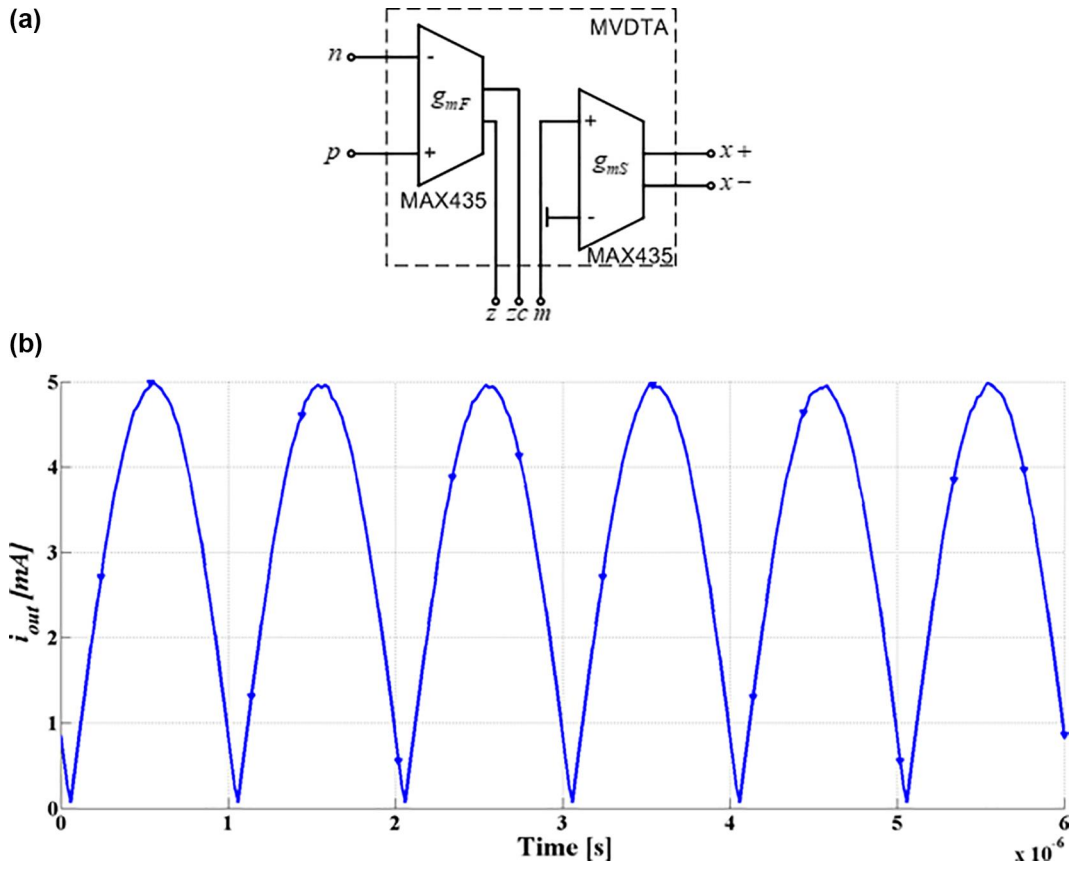

FIGURE 9 (a) Practical implementation of VDTA (b) Experimental result obtained using commercial ICs

TABLE 2 Comparison with previously published rectifiers

Ref.	Type of active building blocks used	Number of diodes	Number of resistors	Max. frequency	Max. amplitude	Power consumption
[2]	1 EXCCII-36 MOS	-	-	125 MHz	±0.5 mA	0.62 mW
[3]	1 EX-CCII-27 MOS	-	-	10 MHz	±200 μA	0.3 mW
[4]	2 VC	2	1	9 MHz	±20 μA	1.38 mW
[5]	1 DO-CCII, MOS Transistors-34	-	1	1 MHz	±100 μA	188 μW
[6]	2 CFOA 3 or 2 NMOS	2	0 or 1	10 MHz	±350mV	1.33 mW
[7]	12 MOS	-	3	85–153.2 MHz	±100 μA	0.16 mW
[8]	1 CCCII-21 (CM) or 23 (VM) MOS	-	-	30 MHz	±500mV (VM) ±1 mA (CM)	1.18 mW (VM) 1.07 mW (CM)
[9]	2 CCII	-	3 (VM) -(CM)	200 kHz	±100 mV (VM) ±200 μA (CM)	-
[16]	1 MOCCCII, CC, 2 (4) MOS	-	-	100 MHz (VM) 200 MHz (CM)	±150 mV (VM) ±300 μA (CM)	4.62 mW
[17]	FDDTA	-	-	50 kHz	±450mV (VM)	8μW
[18]	1 CDTAs	2	1	Variable up to 42 MHz	±5 mA	-
[19]	2 DVCCTA 5 NMOS	-	-	1 MHz	±200 mV	-
[21]	1 CDTA, 2 CMOS	-	1	100 MHz	±200 mV (VM) ±500 μA (CM)	1.12 mW

(Continues)

TABLE 2 (Continued)

Ref.	Type of active building blocks used	Number of diodes	Number of resistors	Max. frequency	Max. amplitude	Power consumption
[24]	1 OTA (1 DVCC)	2 (2)	2 (3)	1 MHz	±300 μA (CM)	-
[25]	2 DVCC	2	2	1 MHz	±150 mV (VM)	0.93 mW
[26]	1 CCII, 28 MOS	-	1	100 MHz	±300 mV (VM)	5.2 mW
[27]	1 MZC-CDTA, MOS Transistors	-	-	10 kHz	±300 μA (CM)	14 mW
[28]	2 CCII	2	3	1 MHz	±150mV (VM)	-
[29]	7 MOS	-	-	20 MHz	±300 μA (CM)	0.150 mW
[30]	4 CCCII	-	6	100 kHz	±500 mV (TC)	-
[31]	OTRA (6 MOS)	1	4	5 MHz	±100 μA (TR)	2.31 mW
[32]	1 CCII, 1 DVCC, 1 MOS	-	4	1 MHz	±20 mV	-
[33]	1 OTA/1 DVCC	2	Two-thirds	1 MHz	±200 μA	-
[34]	1 EX-CCII-24 MOS	-	1	5 MHz	±150 mV	1.7 mW
[35]	2 CCII	2	3	10 MHz	±1V	-
[36]	1 CCII, 1 DXCCII	2	2	10 MHz	±350mV	-
[37]	1 DXCCII, 2 MOS	-	2	50 MHz	±400 mV	≈1.4 mW
[38]	5 MOSFET	4 (MOSFET)	-	20 MHz	2 V	-
[39]	1 CCII	2	2	600 kHz	±350 mV	-
[40]	3 OTRA 6 MOS	-	8	1 kHz	±2 V	-
[41]	DDCC, 2 MOS	-	3	200 MHz	±300 μA	2.94 mW
[42]	EXCCII, 2 MOS	-	-	30 MHz	±300 μA	0.2 mW
This work	1 MVDTA, four NMOS-19 MOS	-	-	50 MHz	±350mV (VM) ±10 mA (CM)	0.84 mW

Abbreviations: CDTA, current differencing transconductance amplifier; DDCC, differential difference current conveyor; DVCC, differential voltage current conveyor; DVCCTA, differential voltage current conveyor transconductance amplifier; DXCCII, dual-X second-generation current conveyor; EX-CCII, extra-X second-generation current conveyor; FDDTA, fully differential difference transconductance amplifier; MZC-CDTA, modified Z copy current difference transconductance amplifier.

without a specially added circuit for temperature compensation.

ACKNOWLEDGMENTS

Research was supported by the Ministry of Education, Science and Technological Development, Republic of Serbia, Grant No. 42,009 and 172,057.

CONFLICT OF INTEREST

This manuscript has not been published and is not under consideration for publication elsewhere. There is no conflict of economic interest. It is warranted that the article is the author's original work. This letter can be used as our statement of originality and confirmation that this paper has not been submitted to any other journals.

PERMISSION STATEMENT TO REPRODUCE THE MATERIALS FROM OTHER SOURCES

None.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are openly available in [ieee explore, Elsevier] at http://doi.org/10.1016/j.aeue.2020.153,267; 10.1109/ICTKE47035.2019.8,966,844: 10.1016/j.aeue.2020.153,360; 10.3390/electronics10111262; 10.1080/03,772,063.2020.1,830,861], reference number [1–42].

ORCID

Predrag B. Petrović https://orcid.org/0000-0002-8849-4230

REFERENCES

1. Sedra, A.S., et al.: Microelectronic circuits, 8th ed, pp. 1086–1087. Oxford University Press, Oxford (2019)
2. Das, R., Paul, S.K.: Resistorless current mode precision rectifier using EXCCII. Analog Integr. Circuits Signal Process. 103, 511–522 (2020)
3. Agrawal, D., Maheshwari, S.: Current-mode precision full-wave rectifier circuits. Circ. Syst. Signal Process. 36, 4293–4308 (2017)
4. Safari, L., et al.: A new versatile full wave rectifier using voltage conveyors. AEU - Int. J. Electron. Commun. 122, 153267 (2020). https://doi.org/10.1016/j.aeue.2020.153267

5. Safari, L., Yuce, E., Minaei, S.: A new low-power current-mode MOS only versatile precision rectifier. AEU - Int. J. Electron. Commun. 83, 40–51 (2018)
6. Yuce, E., Minaei, S., Ibrahim, M.A.: A novel full-wave rectifier/sinusoidal frequency doubler topology based on CFOAs. Analog Integr. Circ. Sig. Process. 93, 351–362 (2017)
7. Srivastava, R., et al.: Low-voltage low-power high performance current mode fullwave rectifier. Microelectron. J. 61, 51–56 (2017)
8. Petrović, P.B.: Current/voltage mode full-wave rectifier based on a single CCCII. Int. J. Circ. Theor. Appl. 48(7), 1140–1153 (2020)
9. Nonthaputha, T., Kumngern, M.: CMOS programmable full-wave rectifier using current conveyor analogue switches. 2019 17th International Conference on ICT and Knowledge Engineering (ICT&KE), pp. 1–5. Bangkok (2019). https://doi.org/10.1109/ICTKE47035.2019.8966844
10. LTC 6268-10/LTC 6269-10, 4GHz Ultra-Low Bias Current FET Input Op Amp, Linear Technology, data-sheets, (2015)
11. Biolek, D., et al.: Active elements for analog signal processing: classification, review, and new proposals. Radioengineering. 17(4), 15–32 (2008)
12. Petrović, P.B.: Tuneable flux-controlled floating memristor emulator circuits. IET Circuits, Devices Syst. 13(4), 479–486 (2019)
13. Petrović, P.B.: New current-mode RMS-to-DC converter and four-quadrant multiplier/divider based on VDTA. IET Circuits, Devices Syst. 14(4), 490–497 (2020)
14. Srivastava, M., Prasad, D., Bhaskar, D.R.: New electronically tunable grounded inductor simulator employing single vdta and one grounded capacitor. J. Eng. Sci. Technol. 12(1), 113–126 (2017)
15. Choubey, C.K., Paul, S.K.: Implementation of chaotic oscillator by designing a simple Chua's diode using a single VDTA. AEU - Int. J. Electron. Commun. 124, 153360 (2020). https://doi.org/10.1016/j.aeue.2020.153360
16. Petrović, P.B.: Variable mode CMOS full-wave rectifier. Analog Integr. Circ. Sig. Process. 90(3), 659–668 (2017)
17. Khateb, F., et al.: Low-voltage diode-less rectifier based on fully differential difference transconductance amplifier. J. Circ. Syst. Comput. 26(11), 1750172 (2017)
18. Khateb, F., Vavra, J., Biolek, D.: A novel current-mode full-wave rectifier based on one CDTA and two diodes. Radioengineering. 19(3), 437–445 (2010)
19. Raj, N., et al.: Electronically tunable full wave precision rectifier using DVCCTAs. Electronics. 10(11), 1262 (2021). https://doi.org/10.3390/electronics10111262
20. Odabasi, I.C., et al.: A Rare Event-Based Yield Estimation Methodology for Analog Circuits. 2018 IEEE 21st International Symposium on Design and Diagnostics of Electronic Circuits & Systems, pp. 33–38. DDECS (2018). https://doi.org/10.1109/DDECS.2018.00013
21. Kaçar, F., Başak, M.E.: A new mixed mode full-wave rectifier realization with current differencing transconductance amplifier. J. Circ. Syst. Comput. 23(715), 1450101 (2014)
22. Herencsar, N., et al.: New compact VM four-phase oscillator employing only single Z-copy VDTA and all grounded passive elements. ELEKTRONIKA IR ELEKTROTECHNIKA. 19(10), 87–90 (2013)
23. Yesil, A., Babacan, Y., Kacar, F.: Design and experimental evolution of memristor with only one VDTA and one capacitor. IEEE Trans. Comput. Aided Des. Integrated Circ. Syst. 38(6), 1123–1132 (2019)
24. Sagbas, M., Minaei, S., Ayten, U.E.: Component reduced current-mode full-wave rectifier circuits using single active component. IET Circ. Dev. & Sys. 10(1), 1–11 (2016)
25. Ibrahim, M.A., Yuce, E., Minaei, S.: A new DVCC-based fully cascadable voltage-mode full-wave rectifier. J. Comput. Electron. 15, 1440–1449 (2016)
26. Kumngern, M.: New versatile precision rectifier. IET Circ. Dev. & Sys. 8(2), 141–151 (2014)
27. Pandey, N., Pandey, R.: Current mode full-wave rectifier based on a single MZCCDTA. Act. Passive Electron. Components. 2013(5). 967057 (2013)
28. Koton, J., Herenscar, N., Vrba, K.: Current and voltage conveyors in current and voltage-mode precision full-wave rectifiers. Radioengineering. 20(1), 19–24 (2011)
29. Yuce, E., Alpaslan, H.: A CMOS current rectifier configuration suitable for integration. J. Circ. Syst. Comput. 21(7), 1250052 (2012)
30. Anuntahirunrat, K., et al.: Sinusoidal frequency doubler and full-wave rectifier based on translinear current-controlled current conveyors. Int. J. Electron. 91(4), 227–239 (2004)
31. Chien, H.C.: Full-phase operation transresistance-mode precision full-wave rectifier designs using single operational transresistance amplifier. Act. Passive Electron. Compon. 2019, 18. 1584724 (2019)
32. Beg, P., Khan, I.A., Maheshwari, S.: Biphase amplifier based precision rectifiers using current conveyors. Int. J. Comput. Appl. 42(3), 14–18 (2012)
33. Koton, J., et al.: Current-mode dual-phase precision full-wave rectifier using current-mode two-cell winner-takes-all (WTA) circuit. Radioengineering. 20(2), 428–432 (2011)
34. Maheshwari, S.: Voltage-mode full-wave precision rectifier and an extended application as ASK/BPSK circuit using a single EXCCII. AEU - Int. J. Electron. Commun. 84(2), 234–241 (2018)
35. Monpapassorn, A.: Low output impedance dual CCII full-wave rectifier. Int. J. Electron. 100(5), 648–654 (2013)
36. Koton, J., Vrba, K., Herencsar, N.: Voltage-mode full-wave rectifier based on DXCCII. Analog Integr. Circ. Sig. Process. 81, 99–107 (2014)
37. Kumar, A., Chaturvedi, B.: Realization of ASK/BPSK modulators and precision full-wave rectifier using DXCCII. AEU - Int. J. Electron. Commun. 99, 146–152 (2019)
38. Jain, P., Joshi, A.: Full-wave bridge rectifier with CMOS pass transistors configuration. J. Circ. Syst. Comput. 27(617), 1850092 (2018)
39. Yildiz, M., Minaei, S., Yuce, E.: A high-performance full-wave rectifier using a single CCII-, two diodes, and two resistors. Sci. Iran. D. 24(6), 3280–3286 (2017)
40. Oruganti, S., et al.: New topologies for OTRA based programmable precision half-wave and full-wave rectifiers. In: Proceedings of the 2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE), pp. 327–331. Noida (2017)
41. Kumari, S., Nand, D.: Current-mode positive and negative rectifier based on DDCC suitable for higher frequency operations. IOP Conf. Ser. Mater. Sci. Eng. 1084, 012079 (2021)
42. Kumar, A., Chaturvedi, B.: Current-mode MOS only precision full-wave rectifier. IETE J. Res. 1–10 (2020). https://doi.org/10.1080/03772063.2020.1830861

How to cite this article: Petrović, P.B.: New full-wave rectifier based on modified voltage differencing transconductance amplifier. IET Circuits Devices Syst. 1–15 (2021). https://doi.org/10.1049/cds2.12106